GaN Systems

GN012 Application Note

Gate Driver Circuit Design with GaN E-HEMTs

March 08, 2022

GaN Systems Inc.

Simple-driven GaN Technology

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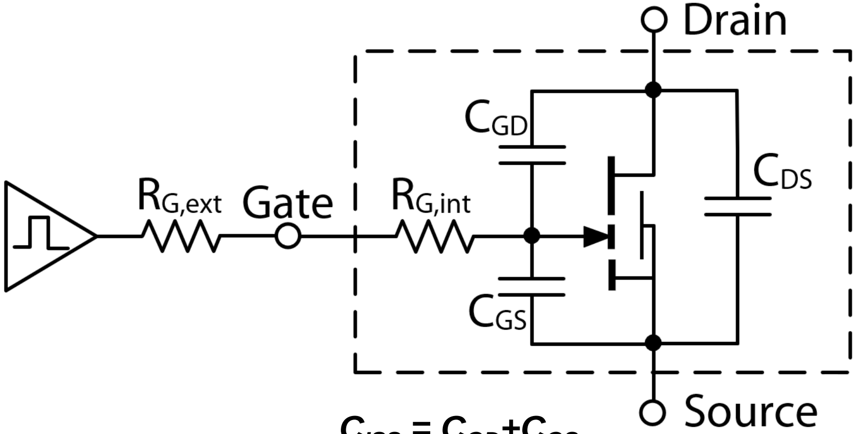
Common with Si MOSFET

- True enhancement-mode normally off
- Voltage driven - driver charges/discharges C_{ISS}
- Supply Gate leakage I_{GSS} only
- Easy slew rate control by R_G
- Compatible with Si gate driver chip



$C_{ISS} = C_{GD}+C_{GS}$

Differences

- Much Lower Q_G : Lower drive loss; faster switching
- Higher gain and lower V_{GS} : +5-6V gate bias to turn on
- Lower $V_{G(th)}$: typ. 1.5V

Versus other enhancement-mode GaN

- More robust gate: -20/+10V max rating
- **No DC gate drive current required**
- **No complicated gate diode / PN junction**

Gate Bias Level	GaN Systems GaN E-HEMT	Si MOSFET	IGBT	SIC MOSFET
Maximum rating	-20/+10V	-/+20V	-/+20V	-8/+20V
Typical gate bias values	0 or-3/+5-6V	0/+10-12V	0 or -9/+15V	-4/+15-20V

❖ GaN HEMTs are **simple to drive**

650V Drivers

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- GaN Systems GaN HEMTs are compatible with most drivers for silicon devices.
- When the driver supply voltage(V_{DD}) is higher than +6V (the recommended turn-on V_{GS} for GaN), a negative V_{GS} generating circuit is required to convert the V_{GS} into +6/-(V_{DD}-6) V, refer to page 7.
- V_{DD} is recommended to ≤12V.

Most popular solutions:

Gate Drivers		Configuration	Isolation	Notes
SILICON LABS	**Si8271**	Single switch	Isolated	Split outputs
SILICON LABS	**Si8273/4/5**	Half-Bridge	Isolated	Dead time programmability
ANALOG DEVICES	**ADuM4121ARIZ**	Single Switch	Isolated	Internal miller clamp
BROADCOM	**ACPL-P346**	Single Switch	Isolated	Internal miller clamp
HEYDAY INTEGRATED CIRCUITS	**HEY1011**	Single Switch	Isolated	Power Rail Integrated
ON Semiconductor	**NCP51820**	Half Bridge	Non-Isolated	Bootstrap voltage management
RENESAS	**RAA226110**	Single Switch	Non-Isolated	Programmable Source Current and Adjustable Overcurrent Protection

100V/80V Drivers

- GaN Systems GaN HEMTs are compatible with most of the drivers for silicon devices.
- When the driver supply voltage(V_{DD}) is higher than +6V (the recommended turn-on V_{GS} for GaN), a negative V_{GS} generating circuit is required to converter the V_{GS} into +6/-(V_{DD}-6) V, refer to page 7.
- V_{DD} is recommended to ≤12V.

Most popular solutions:

Gate Drivers		Configuration	Split Outputs	Bootstrap voltage management	Notes
ON Semiconductor	**NCP51810**	Half-Bridge	Yes	Yes	High Speed
力智電子 POWER INTELLECT	**uP1966A**	Half-Bridge	Yes	Yes	General Purpose
Texas Instruments	**LMG1205**	Half-Bridge	Yes	Yes	General Purpose
MINDCET.	**MDC901**	Half-Bridge	Yes	Yes	High Current

Controllers with Driver Integrated for GaN

- GaN Systems GaN HEMTs are compatible with most of the controllers for silicon devices.
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- V_{DD} is recommended to ≤12V.

Most popular solutions:

Configurations	Controllers	Description
Flyback **- Adapters** **- Chargers** **- Other low-power AC/DCs**	ON Semiconductor **NCP1342**	650V, Quasi-resonant
	Texas Instruments **UCC28600**	600V, Quasi-resonant
	ON Semiconductor **NCP1250**	650V, Fixed frequency
Sync Buck DC/DC (48V/12V)	Analog Devices **LTC7800**	60V, Sync rectifier control, up to 2.2MHz

Controllers with Driver Integrated for GaN - continued

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- GaN Systems GaN HEMTs are compatible with most of the controllers for silicon devices.
- When the driver supply voltage(V_{DD}) is higher than +6V (the recommended turn-on V_{GS} for GaN), a negative V_{GS} generating circuit is required to converter the V_{GS} into +6/-(V_{DD}-6) V, refer to page 7.
- V_{DD} is recommended to ≤12V.

Most popular solutions:

Configurations	Controllers		Notes
LLC - Adapters - Chargers - Flat panel displays - Industrial power	ON Semiconductor	**NCP13992**	600V, current mode controller
	ON Semiconductor	**NCP1399**	600V, current mode controller, off-mode operation
	Texas Instruments	**UCC256404**	600V, optimized burst mode, low audible noise and standby power
	Texas Instruments	**UCC256301**	600V, hybrid hysteric mode, low standby power, wide operating frequency
PFC - PC Power Supplies - Appliances - LED Drivers	ON Semiconductor	**NCP1615 / NCP1616**	700V, critical conduction mode operation
	Texas Instruments	**UCC28180**	Programable frequency, continuous conduction mode operation, no AC line HV sensing
PFC + LLC	MPS Monolithic Power Systems, Inc.	**HR1203**	700V, CCM/DCM Multi-mode PFC control, adjustable dead-time and bust mode switching LLC

Driver Circuit Examples

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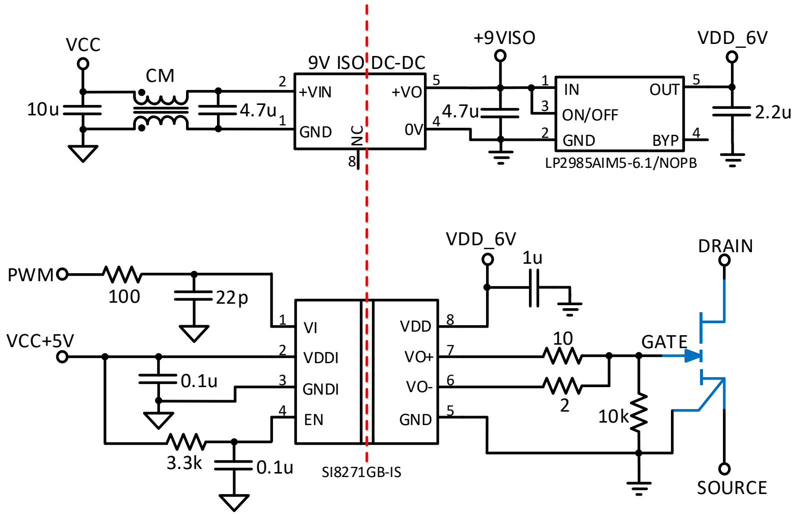
- **Single switch driver**
  - Isolated
    - 0V $V_{GS(OFF)}$ — Single Isolated Driver
    - Negative $V_{GS(OFF)}$
      - EZDrive®
      - With voltage divider
      - Digital Isolator + Non-isolated Driver
  - Non-Isolated
    - 0V $V_{GS(OFF)}$
    - Negative $V_{GS(OFF)}$ — EZDrive®
- **Half/Full Bridge driver**
  - Isolated — Implement two single switch drivers
  - Non-Isolated
    - 0V $V_{GS(OFF)}$ — Bootstrap driver
    - Negative $V_{GS(OFF)}$ — Bootstrap driver + EZDrive®
- **Paralleling GaN**
  - Driver Circuit for GaN HEMT in Parallel

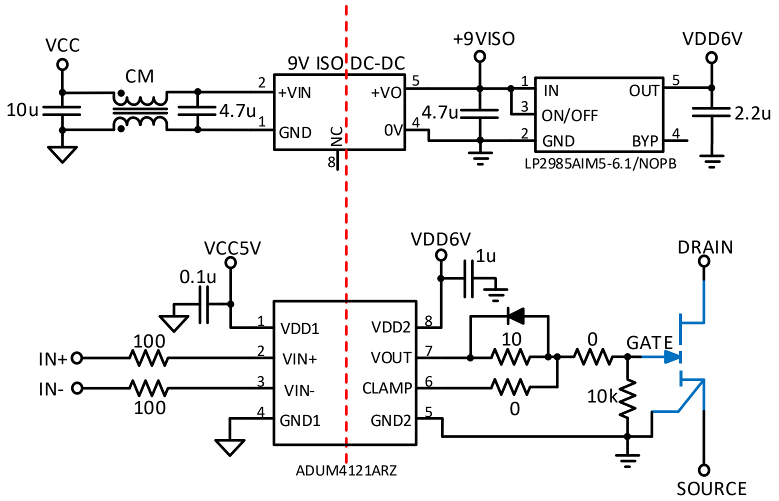
* When is negative $V_{GS(OFF)}$ needed?

Single GaN → Isolated → 0V VGS(OFF) → Single Isolated Driver

- 0V $V_{GS(OFF)}$ for low voltage or low power applications, or where the deadtime loss is critical
- Optional CM Choke for better noise immunity



Example I: Driver with separate outputs for switch ON/OFF (SI8271)



Example II: Driver with single output for switch ON and OFF (ADUM4121)

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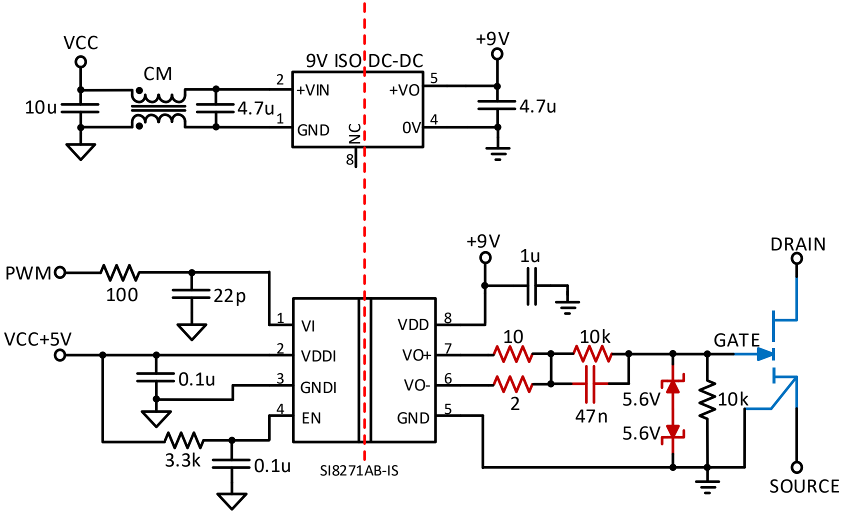
Single GaN → Isolated → Negative $V_{GS(OFF)}$ → EZDrive®

- Negative V_{GS} voltage is applied by the 47nF capacitor
- Compatible with bootstrap circuit
- Applicable from 1kW ~ 100kW power range
- Optional CM Choke for better noise immunity



Example: SI8271 EZDrive® circuit (V_{GS}=+6V/-3V)

For more info about GaN EZDrive®, please refer to GN010: https://gansystems.com/

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Single GaN → Isolated → Negative $V_{GS(OFF)}$ → with Voltage divider

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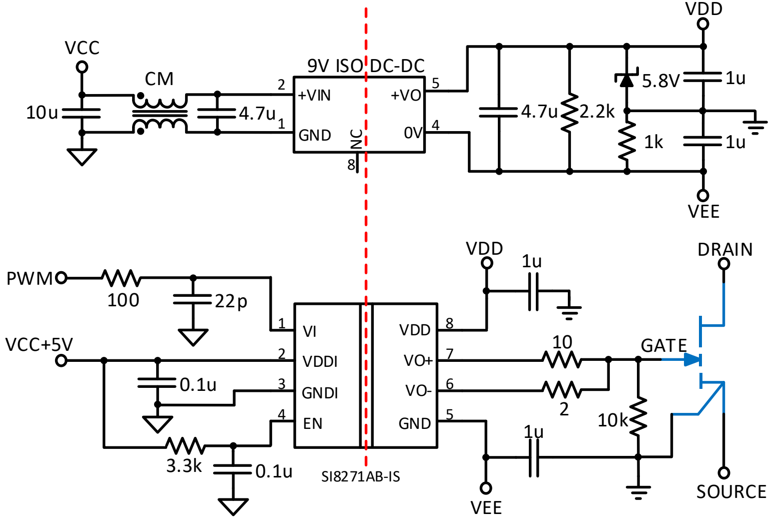
- Negative V_{GS} voltage is generated by the voltage divider (5.8V Zener diode and 1kOhm resistor)
- Robust and easy to layout
- Applicable for applications from low power to higher power (1kW ~ 100kW)
- Optional CM Choke for better noise immunity



Example: SI8271 driving circuit with voltage divider (V_{GS}=+6V/-3V)

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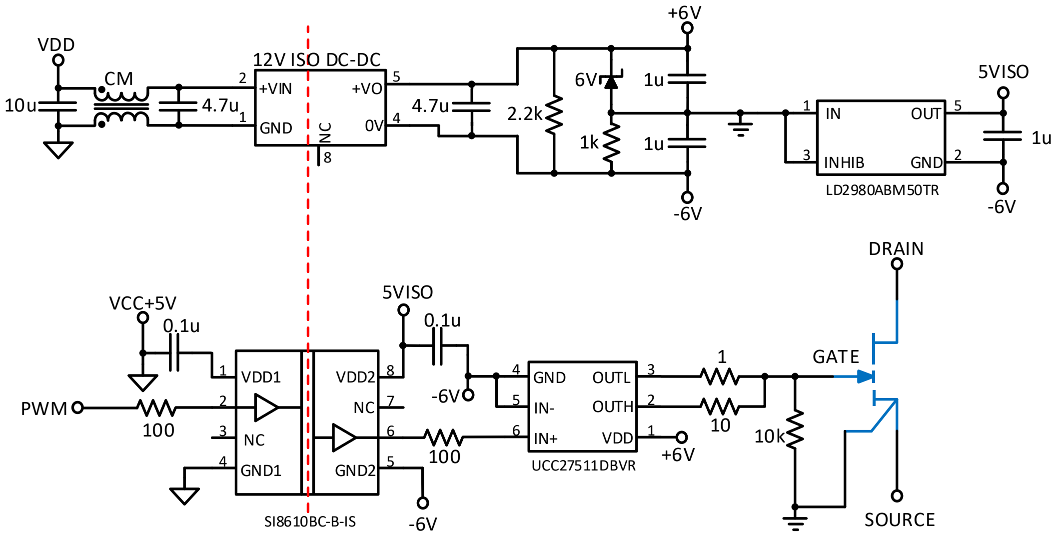
Single GaN → Isolated → Negative $V_{GS(OFF)}$ → Digital Isolator + Non-isolated Driver

- To enable non-isolated driver or buffer with high sink current capability where isolation is required
- For high power applications: e.g. EV motor drive, PV inverter, etc
- Optional CM Choke for better noise immunity



Example: SI8610 (digital isolator) + UCC27511(Non-isolated driver) (V_{GS}=+6V/-6V)

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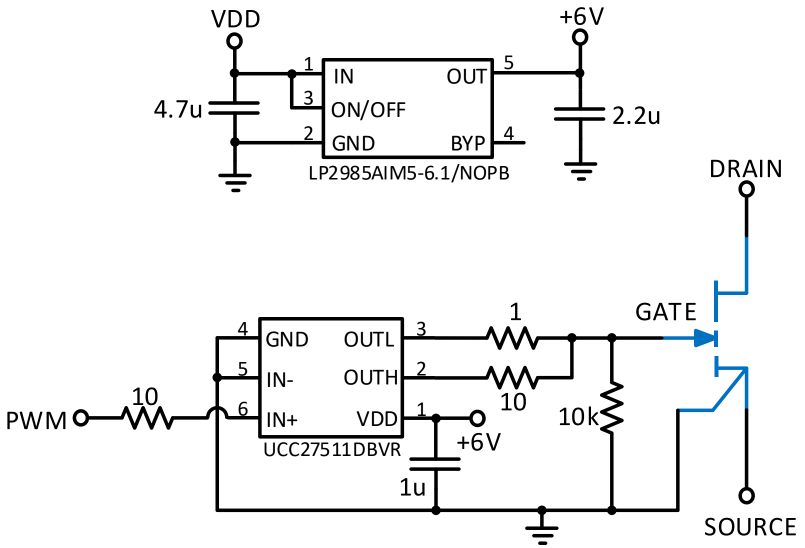
Single GaN → Non-Isolated → 0V $V_{GS(OFF)}$

- For single-ended applications (Class E, Flyback, Push-pull etc)
- Or to work with a digital isolator for the high-side switch



Example: UCC27511 driving circuit (V_{GS}=+6V/0V)

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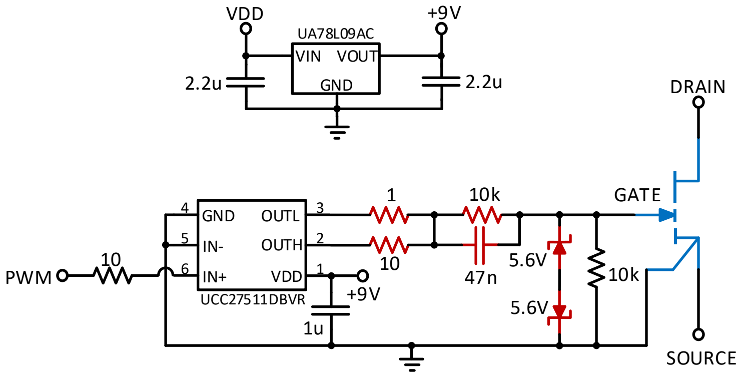
Single GaN → Non-Isolated → Negative $V_{GS(OFF)}$ → EZDrive®

- Negative V_{GS} voltage is applied by the 47nF capacitor
- Compatible with bootstrap circuit
- Optional CM Choke for better noise immunity



Example: UCC27511 driving circuit (V_{GS}=+6V/-3V))

For more info about GaN EZDrive®, please refer to GN010: https://gansystems.com/

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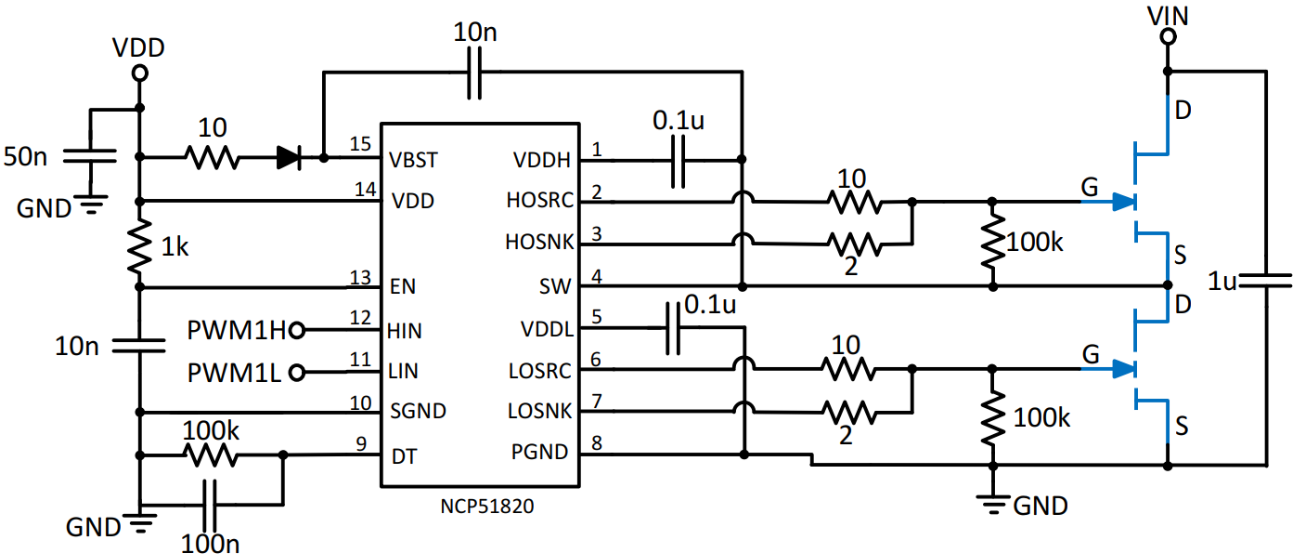
Half/Full Bridge → 0V $V_{GS(OFF)}$ → Bootstrap

- For low power applications
- Choose the bootstrap diode with low C_J and fast recovery time



Example: NCP51820 Bootstrap driving circuit (V_{GS}=+6V/0V)

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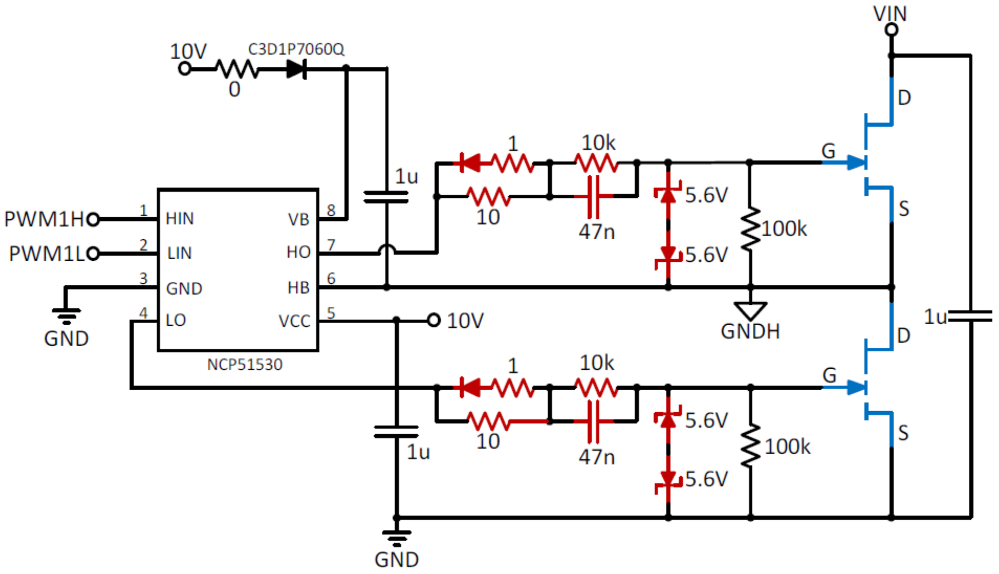
Half/Full Bridge → Negative $V_{GS(OFF)}$ → Bootstrap + EZDrive®

- EZDrive® can get a negative voltage on 47nF capacitor, which can be used as turn off voltage
- Turn on/off slew rate is controllable with external resistors to optimize EMI
- Suitable for low power application



Example: NCP51530 Bootstrap driving circuit with EZdrive® (V_{GS}=+6V/-3V)

For more info about GaN EZDrive®, please refer to GN010: https://gansystems.com/

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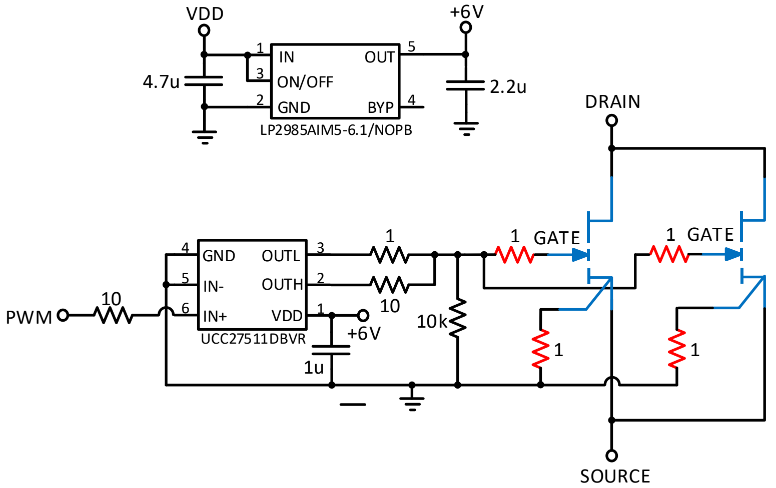
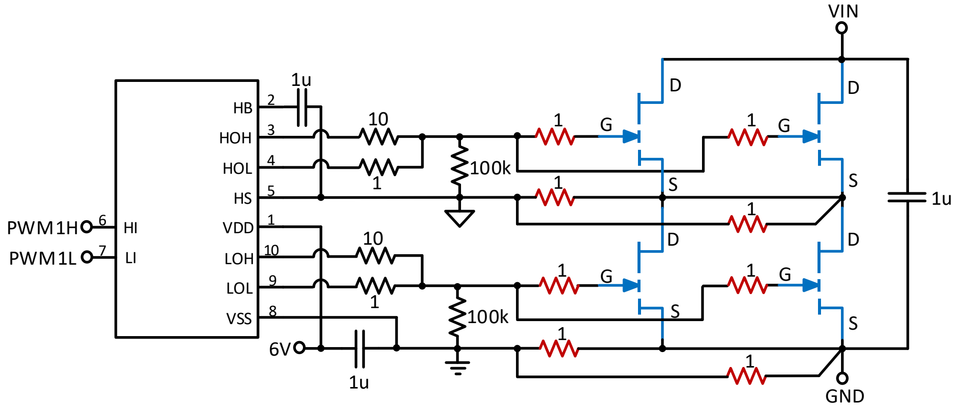
Driver Circuit for GaN HEMT in Parallel

- For HEMTs in parallel, add additional 1ohm gate and source resistors (as highlighted below)



Example: UCC27511 non-isolated driving circuit for single GaN (V_{GS}=+6V/0V)



Example: Bootstrap driving circuit for half-bridge (V_{GS}=+6V/0V)

For more info about GaN in parallel, please refer to GN004: https://gansystems.com/

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Appendix

- Gate driving tips for $V_{GS(OFF)}$
- When is $V_{GS(OFF)}$ needed?
- $V_{GS(OFF)}$ vs. Switching-off Loss
- Trade-off between Switching-off Loss and Deadtime Loss

When is negative $V_{GS(OFF)}$ needed?

- Negative $V_{GS(OFF)}$ can increase noise immunity
- Negative $V_{GS(OFF)}$ can reduce switching-off loss especially under high-current
- Deadtime loss increases as Negative $V_{GS(OFF)}$ increase (more info please refer to page 8, APPNOTE GN001)
- There is a tradeoff between switching-off and deadtime loss for $V_{GS(OFF)}$ selection. -3V $V_{GS(OFF)}$ is recommended to start with for above 0.5kW applications.

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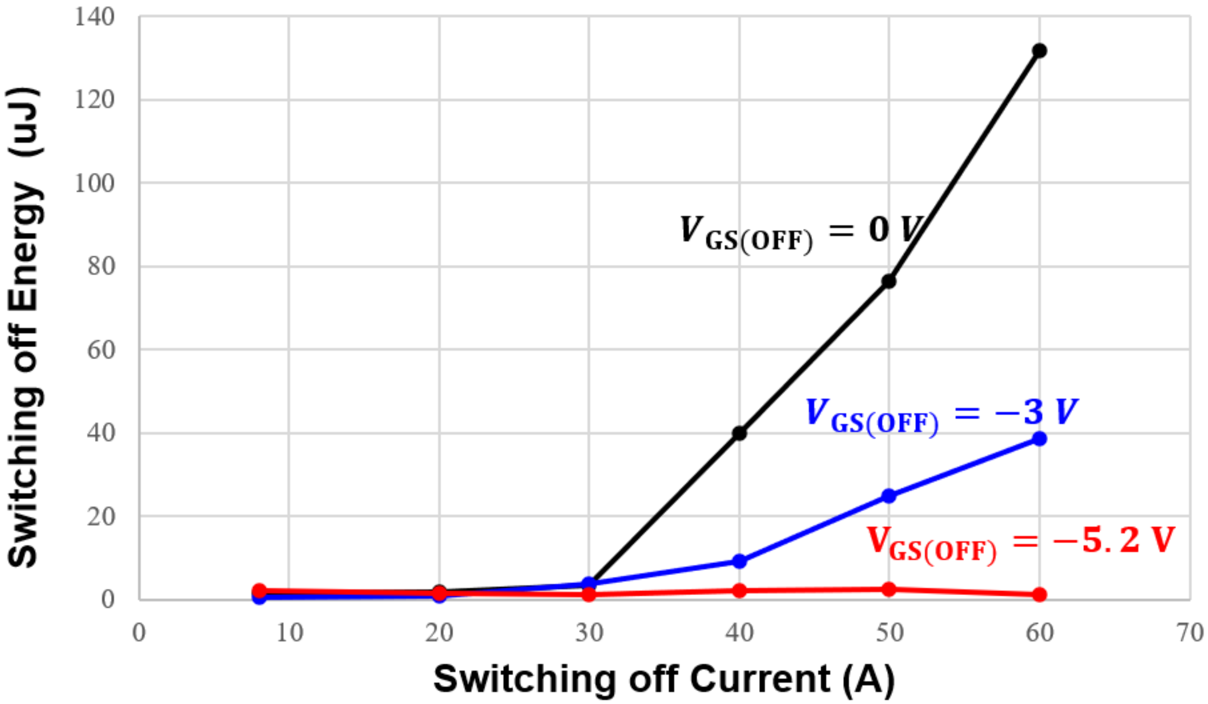
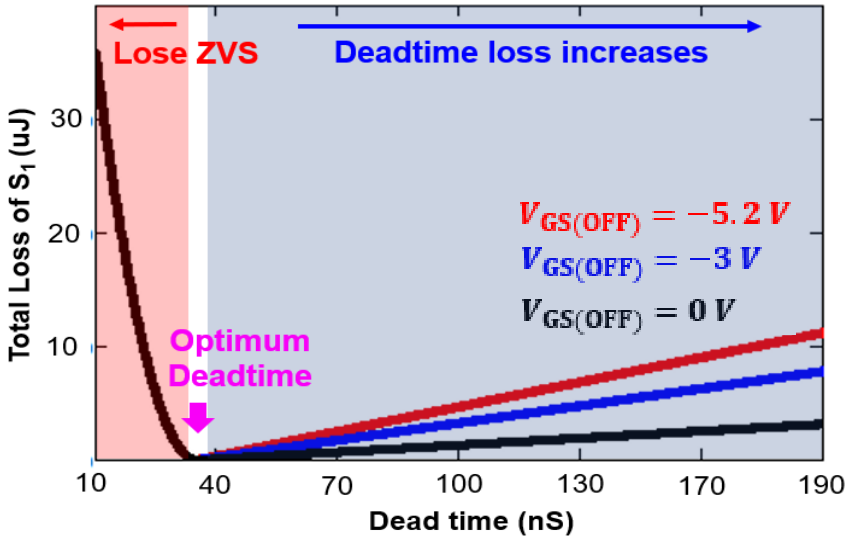
$V_{GS(OFF)}$ vs. Switching-off Loss



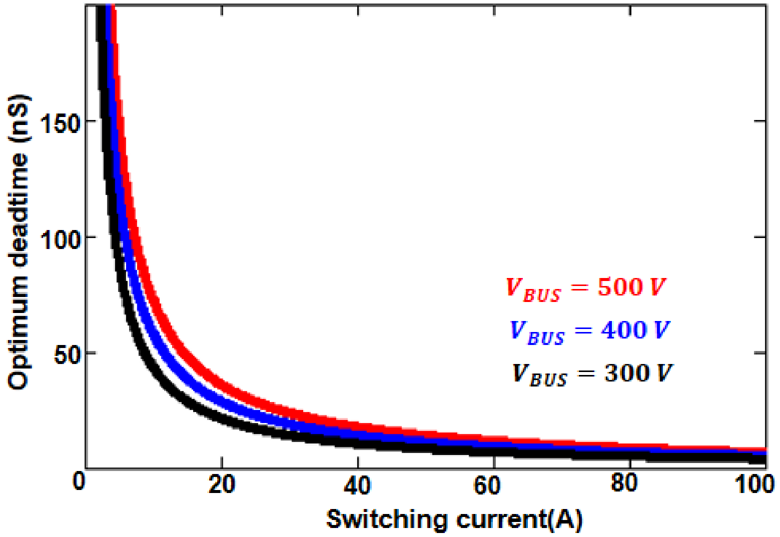
Switching-off loss of GS66516B vs. current at V_{BUS}=400 V, 25°C, R_G=1Ω

Negative V_{DRoff} reduces the switching off energy under high current.

$V_{GS(OFF)}$ vs. Zero Voltage Switching Boundary and Dead Time Loss



Relation between total loss and deadtime of GS66516B at I_D=10A, 25 °C



Optimum deadtime Vs. switching off current at V_{BUS}=400V

ZVS boundary:

$$t_d > \frac{C_{eq} \cdot V_{bus}}{i_{Switching}} \quad (1)$$

$$0.5 \cdot L \cdot i_{Smin}{}^2 > i_{Smin} \cdot V_{SD} \cdot \left(t_d - \frac{C_{eq} \cdot V_{DC}}{i_{Smin}}\right) + 0.5 \cdot C_{eq} \cdot V_{DC}{}^2 \quad (2)$$

- **Deadtime loss increases as $V_{GS(OFF)}$ increases**
- **A too short dead time will result in losing ZVS, while a too long dead time will cause additional loss**

Trade-off between Switching-off Loss and Deadtime Loss

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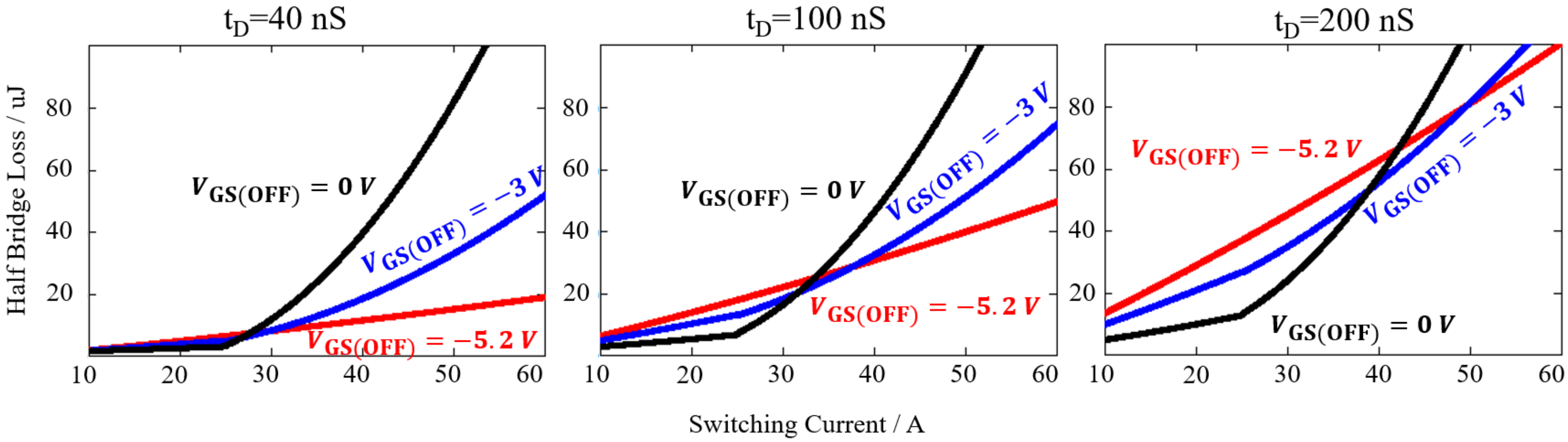

Half-bridge overall loss vs. switching current under different negative turn-off gate voltage V_{DRoff}
(a) with deadtime t_D=40 nS, (b) with deadtime t_D=100 nS, (c) with deadtime t_D=200 nS.

- **Negative V_{DRoff} is will make the power stage more efficient under higher power.**
- **Precise dead time control is the key to higher system efficiency.**

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