



GN008 Application Note

GaN Switching Loss Simulation using LTSpice

March 08, 2022

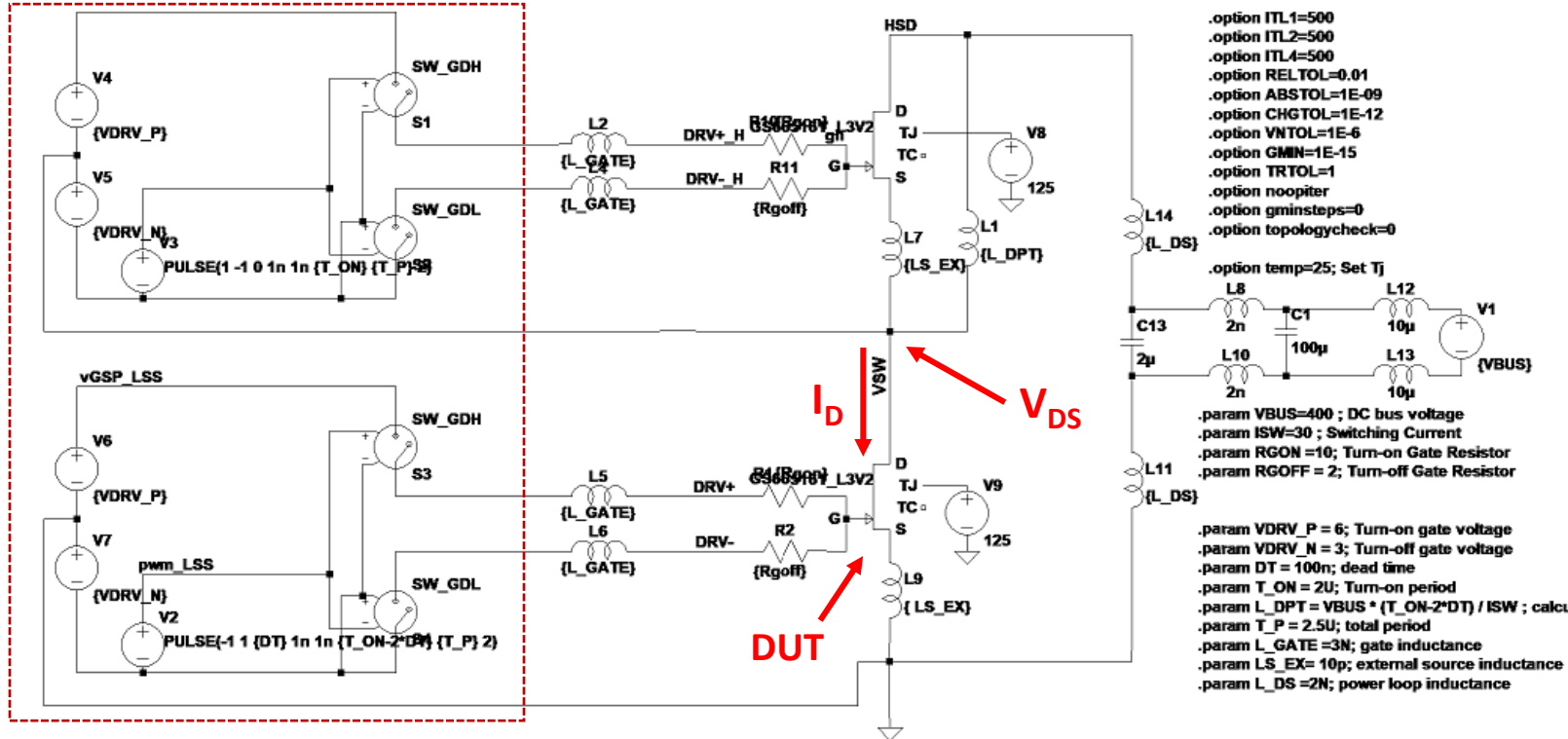
GaN Systems Inc.



- GaN Systems provides Pspice / LTSpice simulation models for GaN Enhancement mode HEMT.
- In this presentation, a half bridge double pulse test circuit in LTSpice is introduced and used as the test bench to evaluate switching performance under different electrical parameters.
- Switching losses were simulated and compared with Lab measurement

GAN SYSTEMS SWITCHING LOSS DOUBLE PULSE TEST BENCH

```
.model SW_GDH VSWITCH Roff=1e6 Ron=2 Voff=0 Von=1
.model SW_GDL VSWITCH Roff=1e6 Ron=.4 Voff=0 Von=1
```



```
.tran 0 3U 0 0.1n
```

```
.option ITL1=500
.option ITL2=500
.option ITL4=500
.option RELTOL=0.01
.option ABSTOL=1E-09
.option CHGTOL=1E-12
.option VNTOL=1E-6
.option GMN=1E-15
.option TRTOL=1
.option noopter
.option gminsteps=0
.option topologycheck=0
```

```
.option temp=25; Set Tj
C13 2u
L8 2n
L10 2n
L12 10u
L13 10u
V1 [VBUS]
```

```
.param VBUS=400 ; DC bus voltage
.param ISW=30 ; Switching Current
.param RGON=10; Turn-on Gate Resistor
.param RGOFF= 2; Turn-off Gate Resistor
```

```
.param VDRV_P = 6; Turn-on gate voltage
.param VDRV_N = 3; Turn-off gate voltage
.param DT = 100n; dead time
.param T_ON = 2U; Turn-on period
.param L_DPT = VBUS * (T_ON-2*DT) / ISW ; calculated L for switching current
.param T_P = 2.5U; total period
.param L_GATE=3N; gate inductance
.param LS_EX= 10p; external source inductance
.param L_DS =2N; power loop inductance
```

HS/LS Gate driver circuit

Set up the simulation parameters:

.option temp=25 ; Junction temperature setting, adjust between 25 and 150C

.param VBUS = 400; DC bus voltage
.param ISW = 30; Switching Current
.param RGON =10; Turn-on Gate Resistor
.param RGOFF = 2; Turn-off Gate Resistor
.param VDRV_P = 6; Turn-on gate voltage
.param VDRV_N = 3; Turn-off negative gate voltage

Switching test parameters

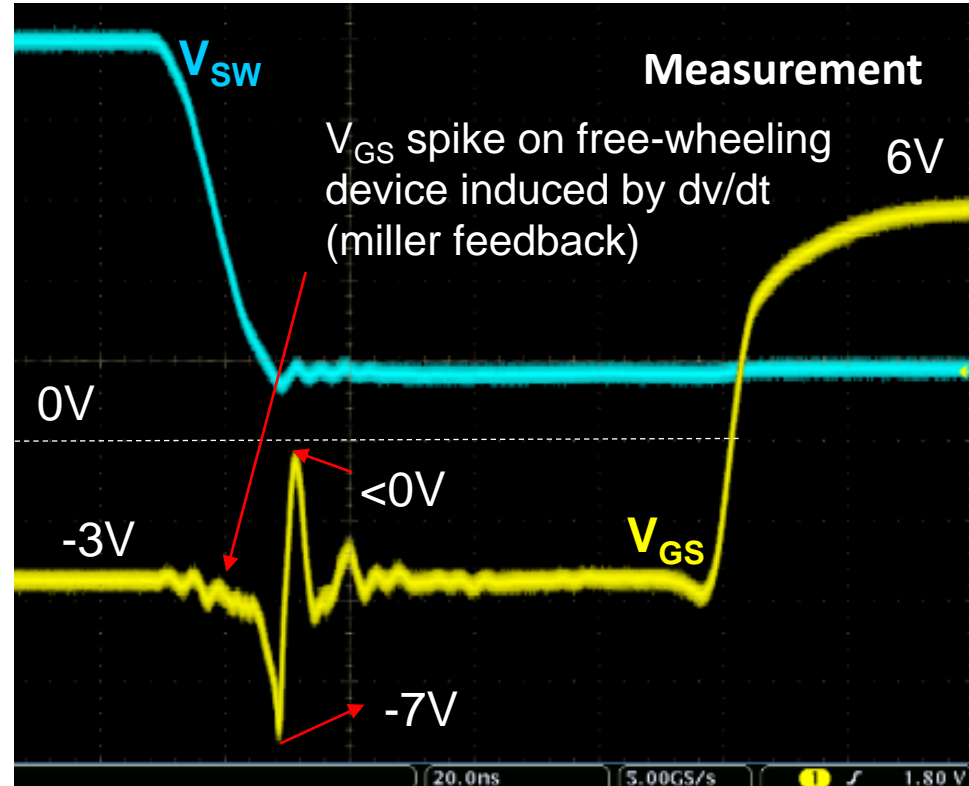
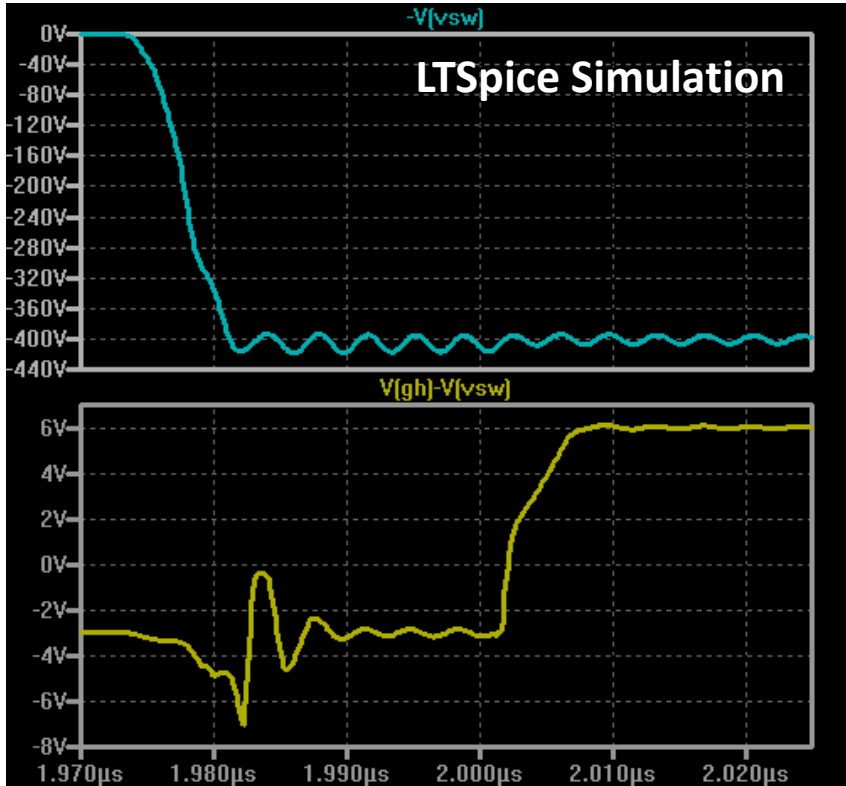
.param DT = 100n; dead time
.param T_ON = 2U; Turn-on period
.param L_DPT = VBUS * (T_ON-2*DT) / ISW ; calculated L for switching current setting

.param T_P = 2.5U; total period
.param L_GATE =3N; gate inductance
.param LS_EX= 10p; external source inductance
.param L_DS =3N; power loop inductance

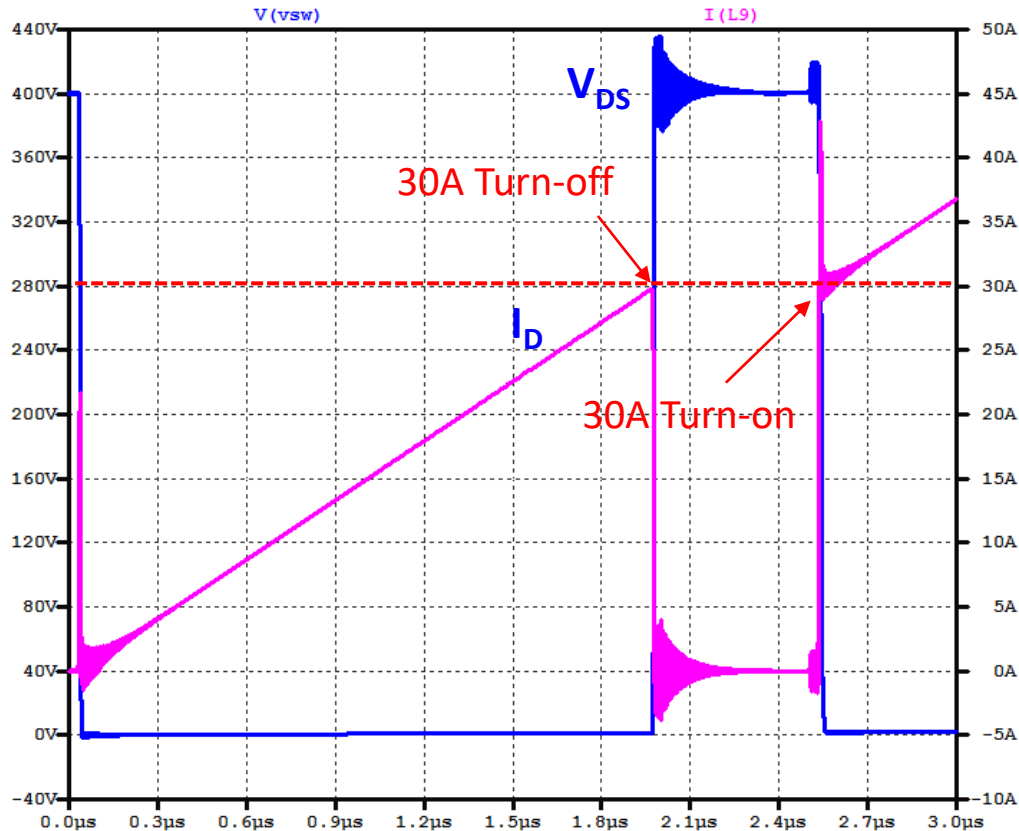
Parasitic Inductances

Gate waveforms (Simulated vs Measured)

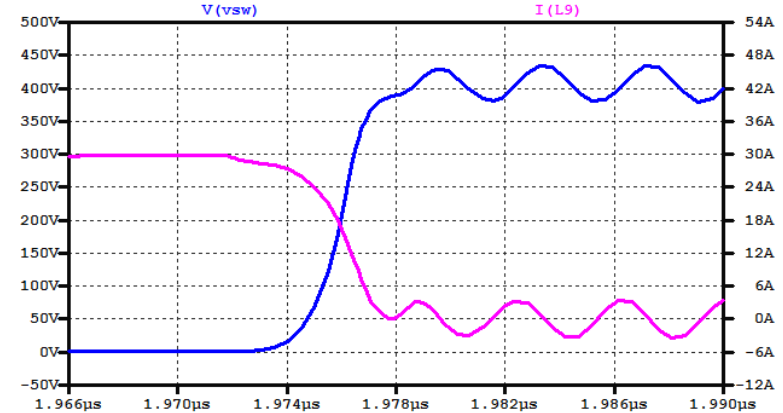
- Good correlation between simulated and measured waveforms.
- Parasitics: $L_{DS} = 3\text{nH}$, $L_{GATE} = 3\text{nH}$



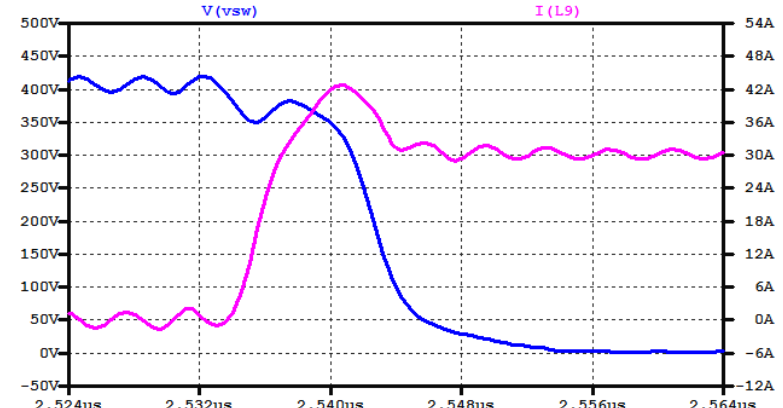
Double Pulse Simulation Results (400V/30A)



400V/30A Hard switch-off

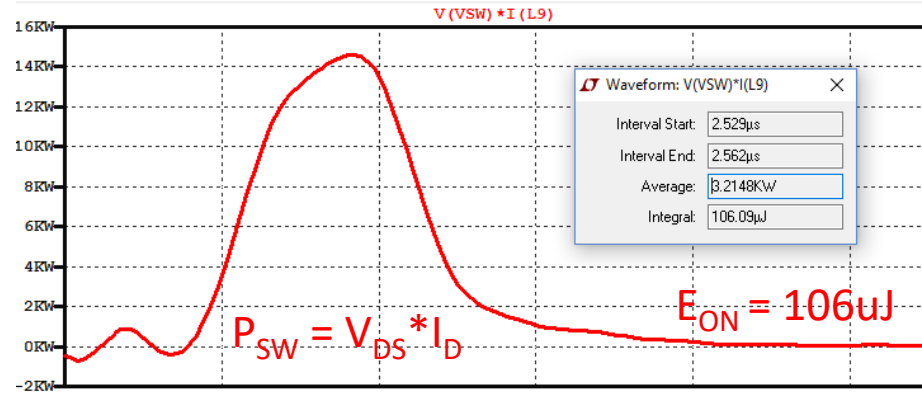


400V/30A Hard switch-on

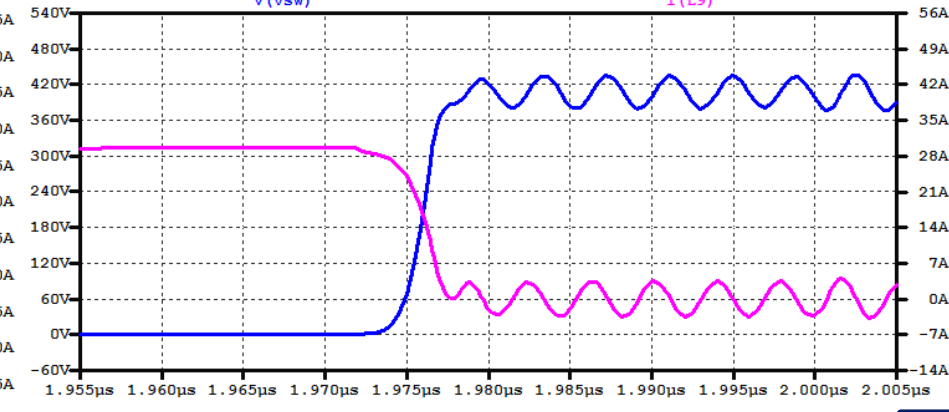
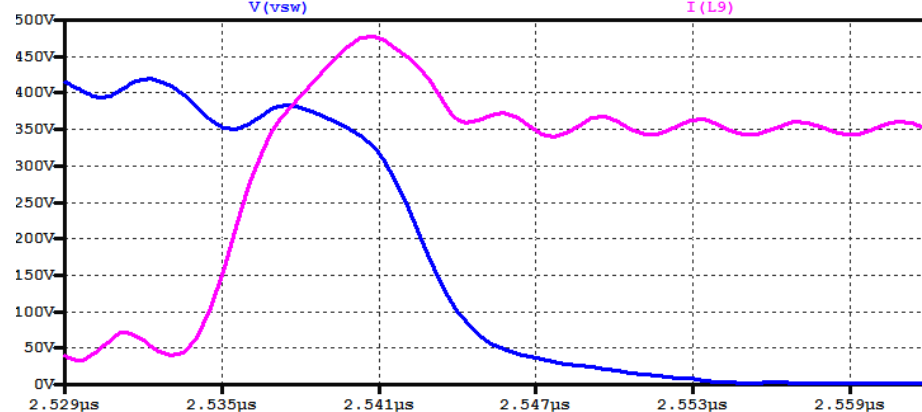
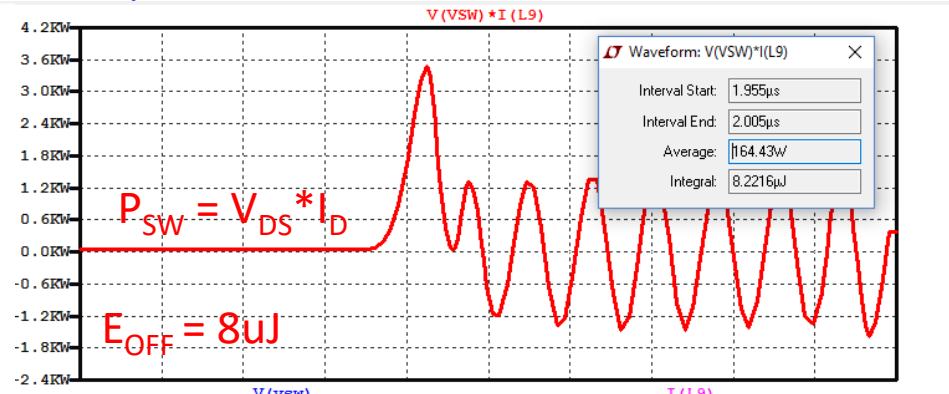


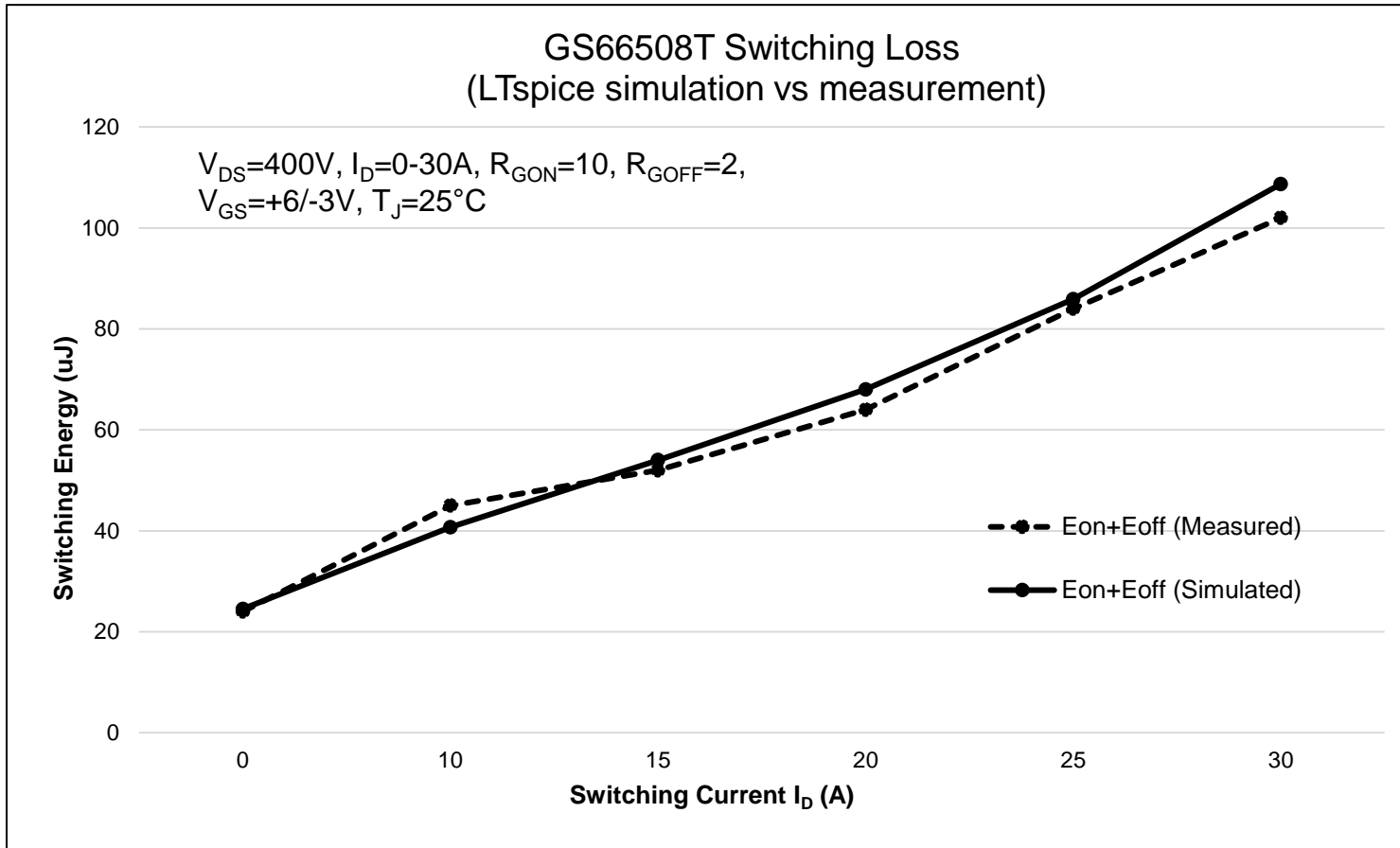
Switching Loss Calculation using LTSpice

400V/30A Turn-on



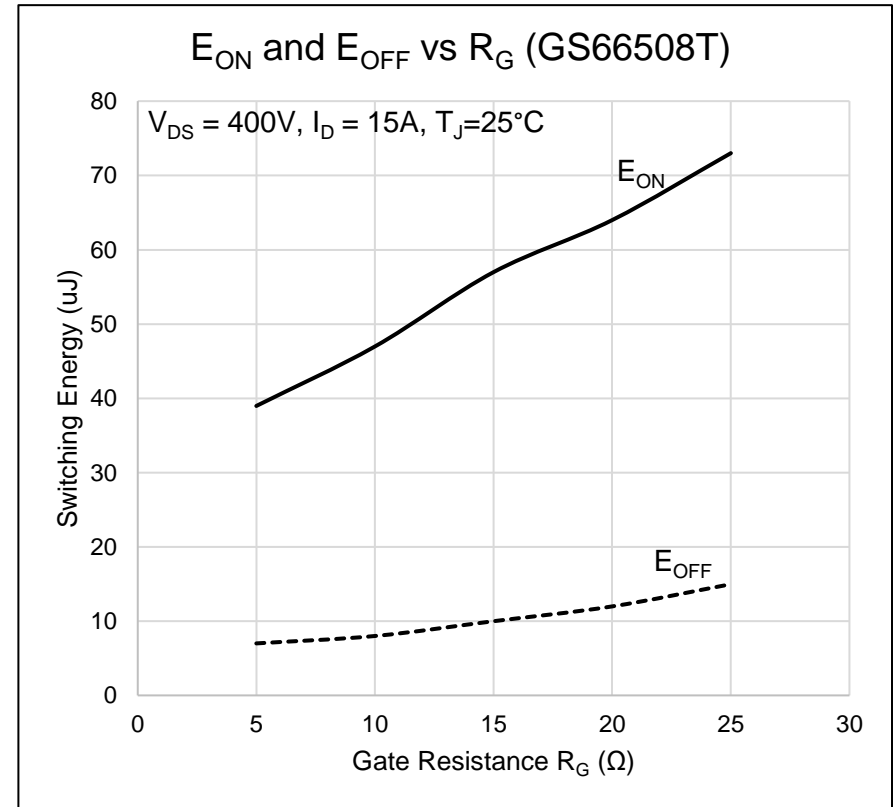
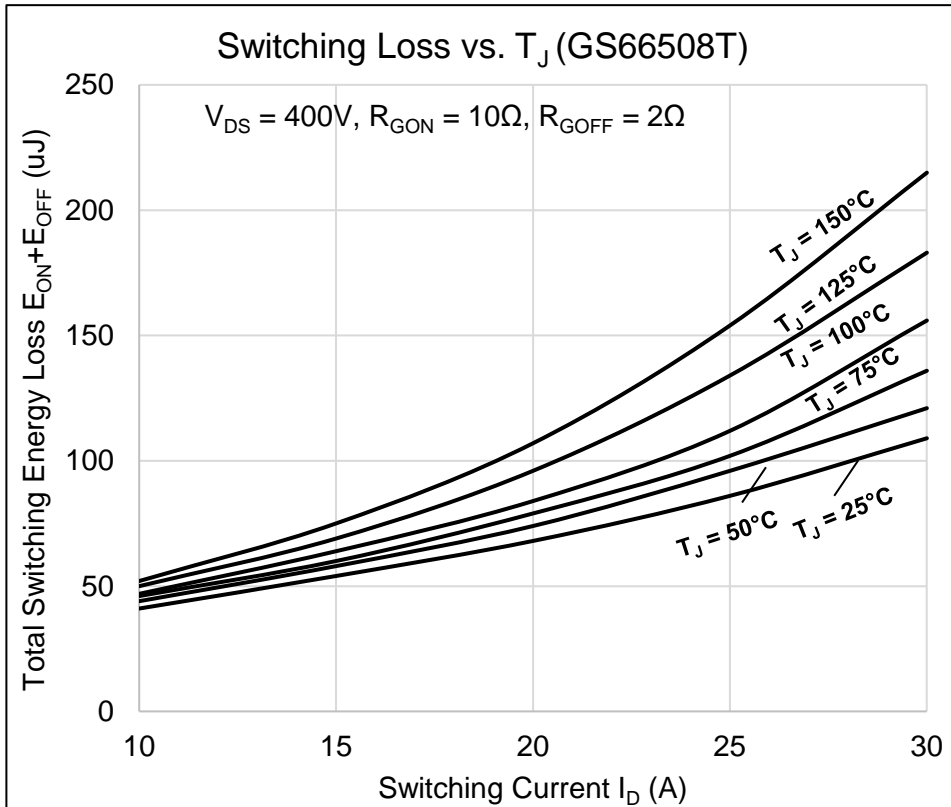
400V/30A Turn-off





- Turn-on loss increases with T_J due to the reduced trans-conductance at higher temperature
- Turn-off loss for GaN is low and less temperature dependent

- Switching Loss increases with R_G .



- The GaN E-HEMT switching losses were simulated in LTSpice using a half bridge double pulse test circuit.
- The simulation results were verified against lab measurements. Although the real world measurement can be affected by many factors, a reasonably good agreement was achieved between the simulation model and measurement data.
- This LTSpice test circuit is a convenient tool for end users to set up a simulation platform and familiarize themselves with with GaN E-HEMT switching characteristics.
- It can also be used to easily evaluate the effects of different electrical parameters on GaN E-HEMT switching performance.

[Click to download LTSpice Simulation File](#)

[Click to download the LTSpice Model User Guide](#)



Product and application support at
gansystems.com