GN004 Application Note

Design Considerations of Paralleled GaN HEMTs

GaN Systems Inc.

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Introduction

Paralleling of switches is necessary in high power applications such as traction inverters, renewable energy systems etc. This application note provides details on the design considerations of GaN FETs in parallel so that designers can release optimized designs and achieve the best system performance.

The benefits of paralleling GaN are discussed. The characteristics of GaN are analyzed and show that GaN is inherently fit for paralleling.

For higher overall system performance, improvements in the design must take place to reduce the impact of parasitics in paralleling layout applications and this is illustrated in this application.

A design example of 4 x paralleled GaN HEMTs is presented and the test results show that the thermal balance of GaN HEMTs is achieved.

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Paralleling GaN **Benefits**

Purpose of Paralleling GaN Transistors

- Paralleling of switches is necessary in high-power handling, high-output current, high-efficiency applications.
- Examples: Traction inverters, renewable energy systems, and uninterruptible power supplies.

Benefits of Paralleling GaN Power Devices

- Improved thermal management
- Redundancy
- Expandability of output power
- Ease in standardization

Characteristics fit for Paralleling

- GaN Systems E-HEMT device characteristics are inherently fit for paralleling
- Loss distributions (conduction & switching losses) of paralleled GaN HEMTs show superior paralleling capability.

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Essential GaN Characteristics – **Good for Paralleling**

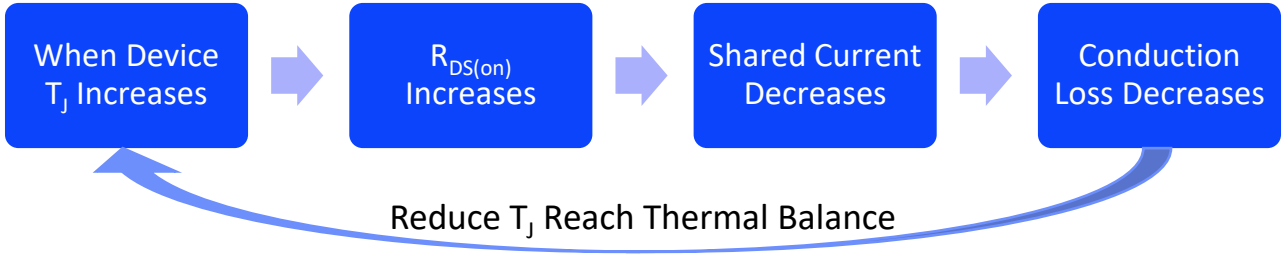
GaN has positive temperature coefficient of $R_{DS(on)}$

GaN has stable gate-source threshold voltage $V_{GS(th)}$ over temperature

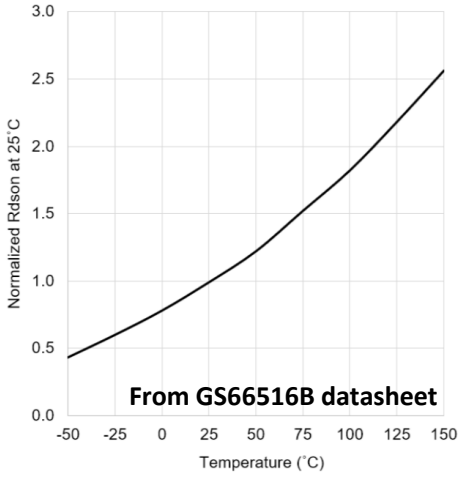
GaN E-HEMT trans-conductance g_m decreases with temperature

2 Conduction Loss Distribution: $R_{DS(on)}$ vs T_J

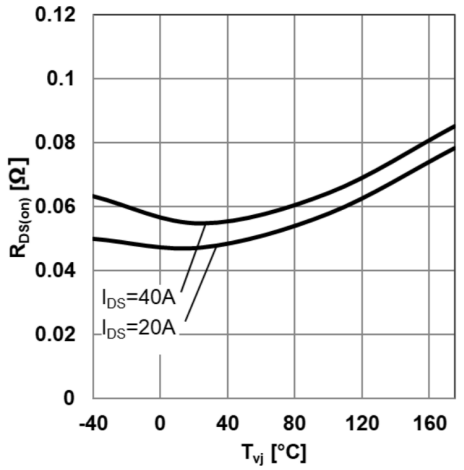
- GaN has **positive** temperature coefficient of $R_{DS(on)}$
- **Positive temperature coefficient** of $R_{DS(on)}$ **helps** the thermal balance in parallel applications:



GaN $R_{DS(on)}$ Temperature Dependence



SiC $R_{DS(on)}$ Temperature Dependence

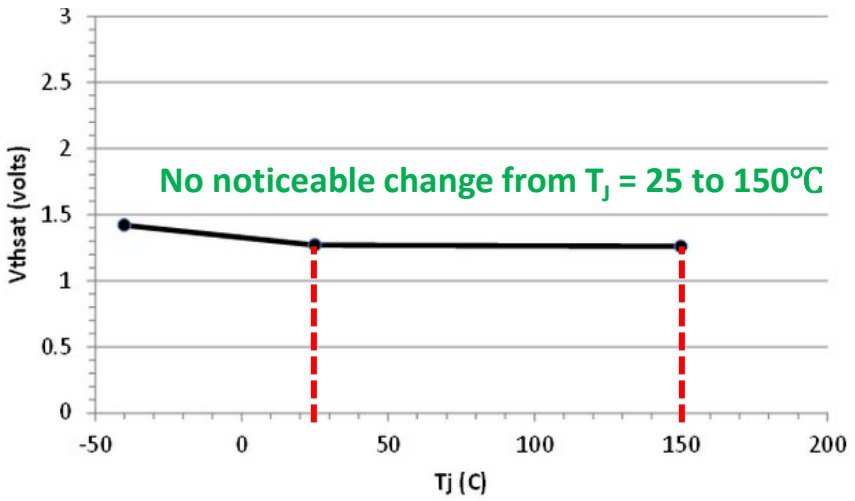


- Compared to SiC, strong $R_{DS(on)}$ temperature dependence of GaN **helps** the current sharing in parallel applications

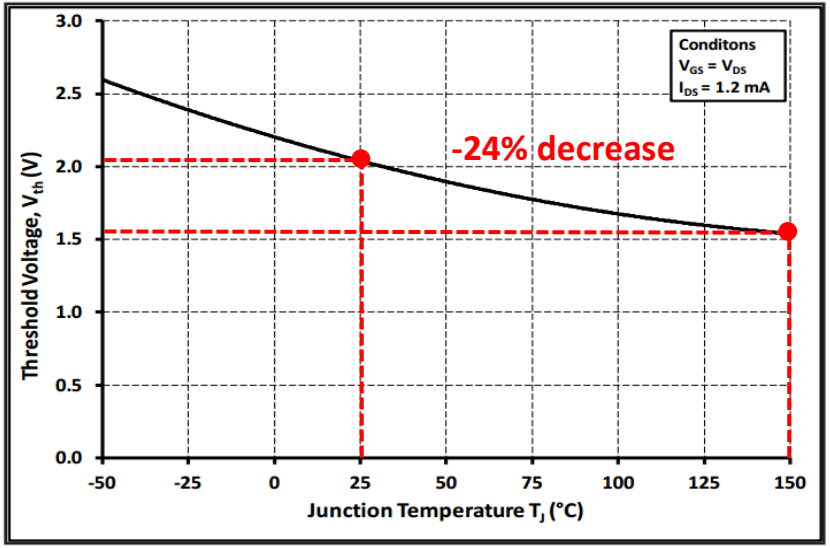
2 Switching Loss Distribution: $V_{GS(th)}$ vs T_J

- In parallel applications, current sharing heavily relies on **stable** gate-source threshold voltage $V_{GS(th)}$
- GaN has **stable** gate-source threshold voltage $V_{GS(th)}$ over temperature as compared to SiC
- GaN has superior paralleling capability

GaN Gate-Source Threshold $V_{GS(th)}$ Temperature Dependence



SiC Gate-Source Threshold $V_{GS(th)}$ Temperature Dependence

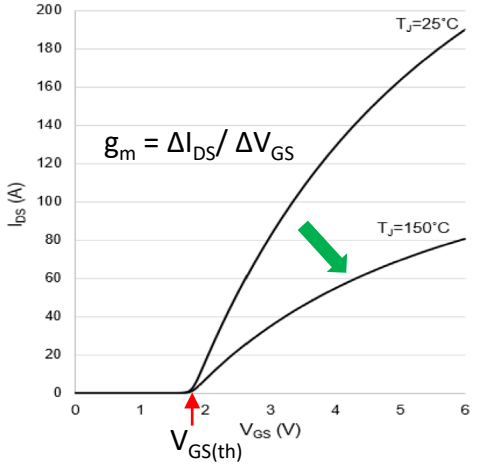
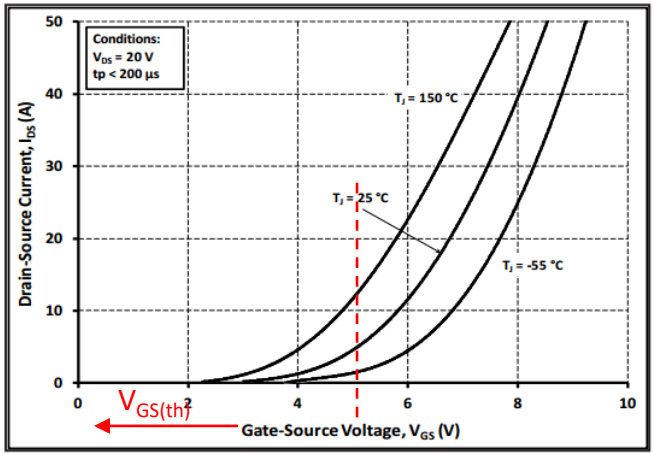
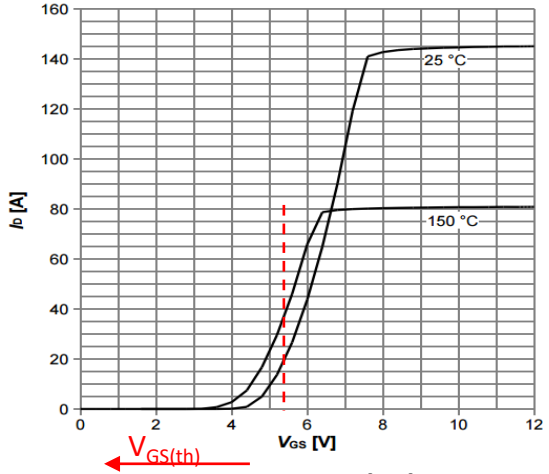


2 Switching Loss Distribution: g_m vs T_J

- GaN E-HEMT trans-conductance g_m decreases with temperature, **good for paralleling**
- **Negative** temperature coefficient of g_m helps the thermal balance in parallel applications:

When Device T_J Increases → $g_{(m)}$ Decreases → Shared Current Decreases → Switching Loss Decreases

Reduce T_J Reach Thermal Balance

GaN g_m Temperature Dependence	SiC g_m Temperature Dependence	Si g_m Temperature Dependence
		
• I_{DS} decreases at same V_{GS} at higher T_J • $V_{GS(th)}$ remains constant at higher T_J	• I_{DS} increases at same V_{GS} at higher T_J • $V_{GS(th)}$ decreases at higher T_J	• gm remains constant at higher T_J • $V_{GS(th)}$ decreases at higher T_J

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3 Key Layout Parameters in Paralleling Applications

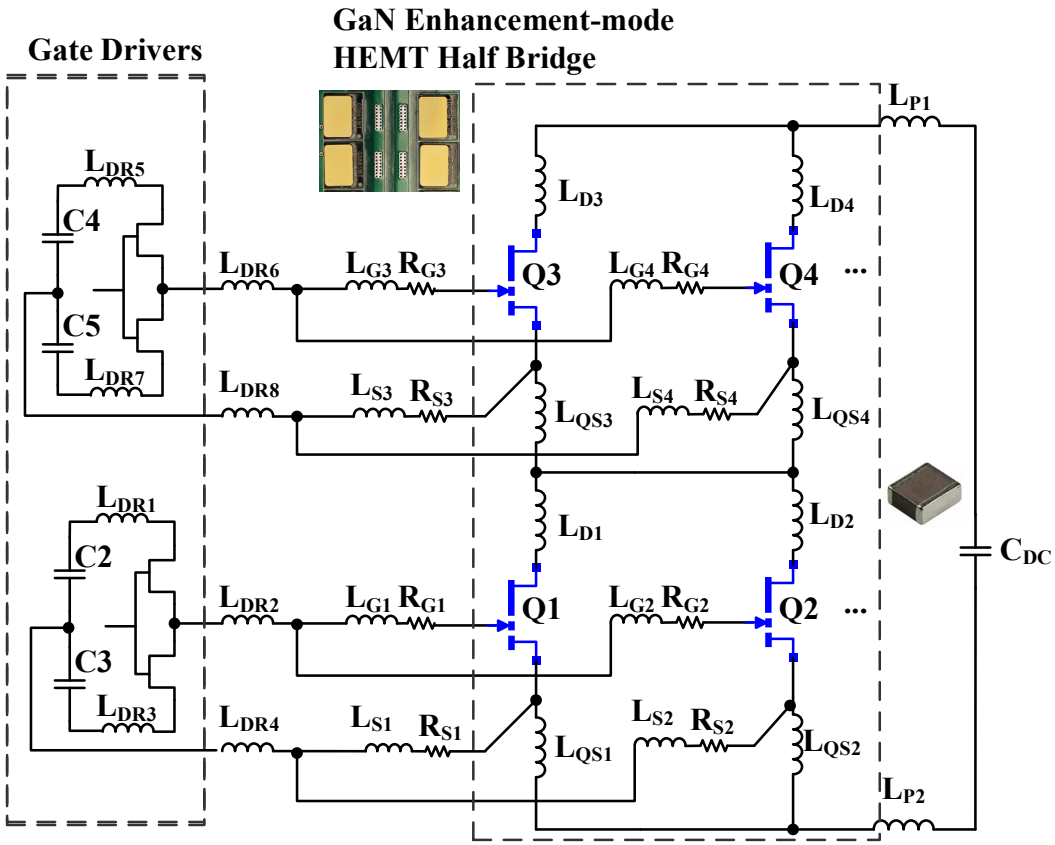
Here are the key layout parasitic parameters, minimize as much as possible to have the optimized system performance:

L_{G1-4} & L_{S1-4}: Gate/Source inductance

- **Equalize L_G/L_S using star connection** and keep as low as possible
- **Individual R_G/R_S** is recommended to reduce gate ringing among paralleled devices

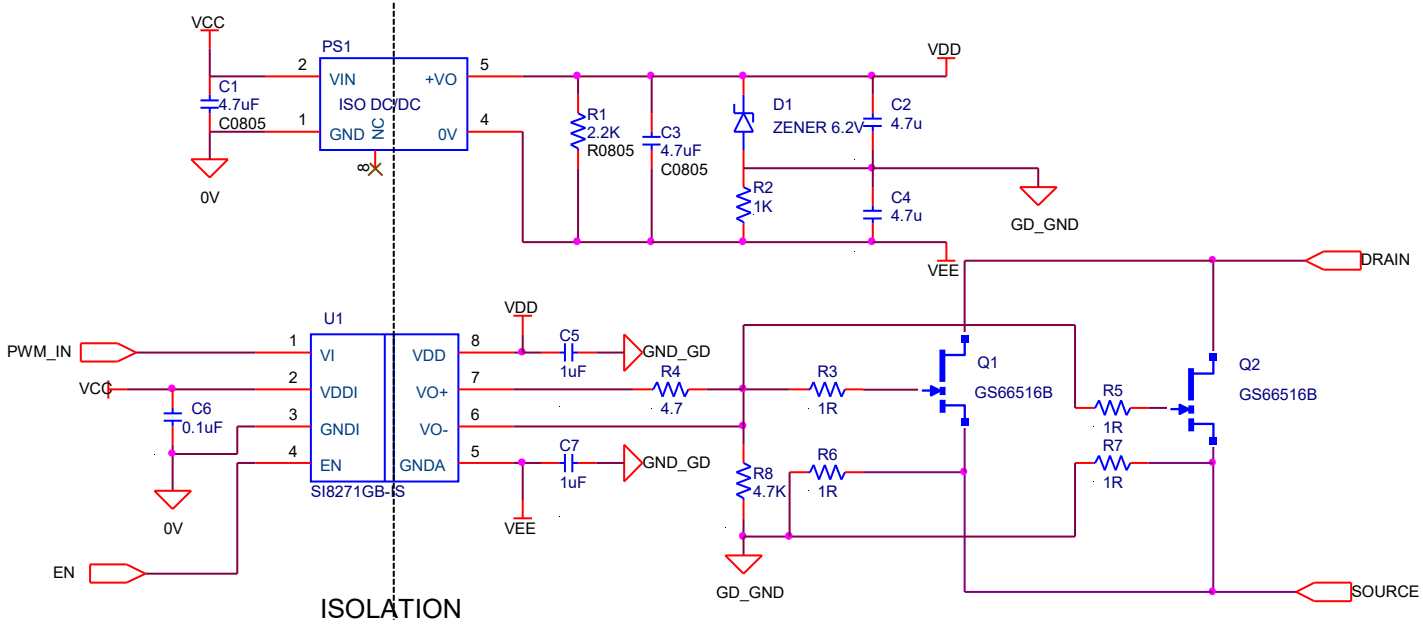
L_{QS1-4} : Common source inductance

- Defined as any inductance that couples power loop switching noise (L*di/dt) into the gate drive circuit, feedback switching di/dt to V_{GS}
- Including the shared/common source inductance and mutual inductance between power and drive loops



Design considerations of gate driver circuit:

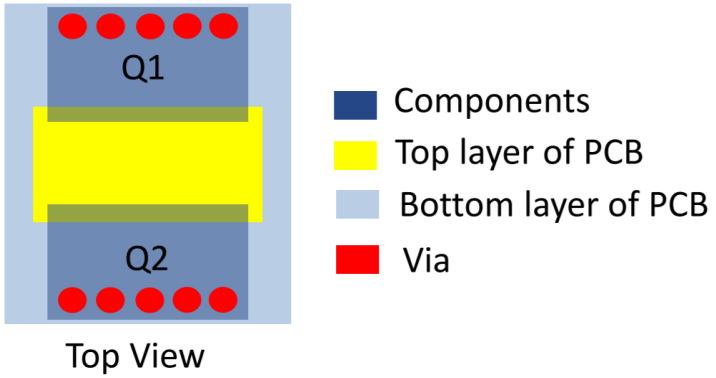
- For high current paralleling design, negative gate drive turn-off bias (-3V to -6V) is recommended for **lower turn-off loss** and **more robust** gate drive
- Create bipolar gate drive from single power supply using a 6.2V Zener (VDD = 6.2V and VEE = 6.2V - PS1 output)
- Distributed gate resistors (R3/R5 = 1-2Ω) and source resistors (R6/R7 = 1-2Ω) are added to **reduce gate ringing** among paralleled devices
- **Minimize** the gate driver loop to reduce its impact on paralleled devices current sharing



Refer to **application note GN009 (PCB Layout Considerations with GaN E-HEMTs) for more information about optimizing the gate driver loop*

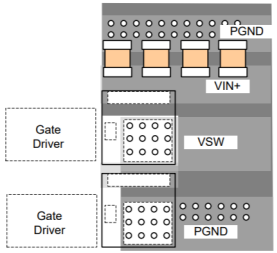
Design considerations of power commutation loop:

- ❑ Minimize the power loop length (including the GaN FETs and decoupling capacitors)
- ❑ To reduce the power commutation loop inductance, it is important to use **magnetic flux cancellation approach**: when two adjacent conductors are located close with opposite current direction, magnetic flux generated by two current flows will cancel each other

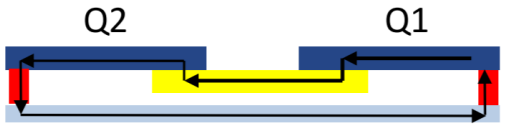


Top View

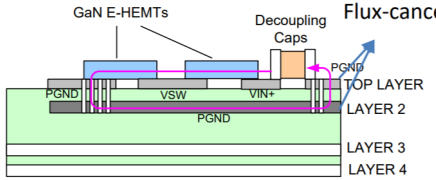
Example: Bottom-side cooled devices
(gate driver/GaN HEMT/caps on the same side of PCB)



Top view



Side View



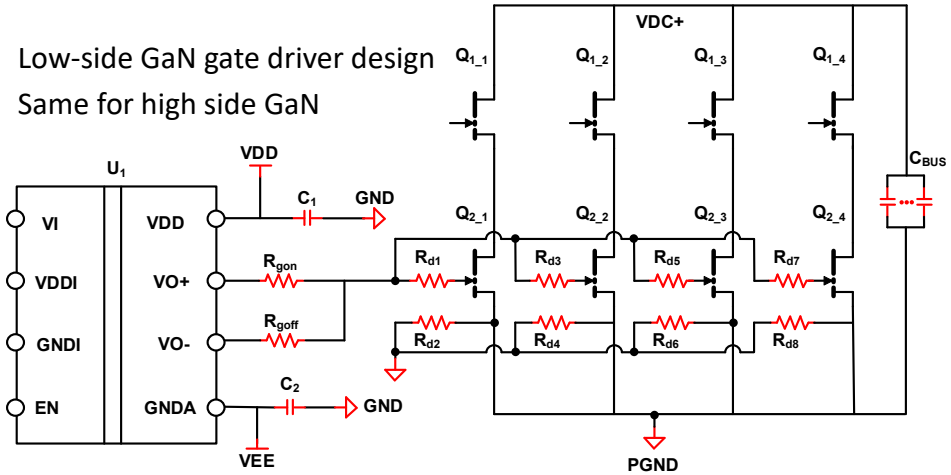
Use layer 2 as ground return (4-layer PCB)

Side view

Design example of 4x top cooled GaN FETs in parallel:

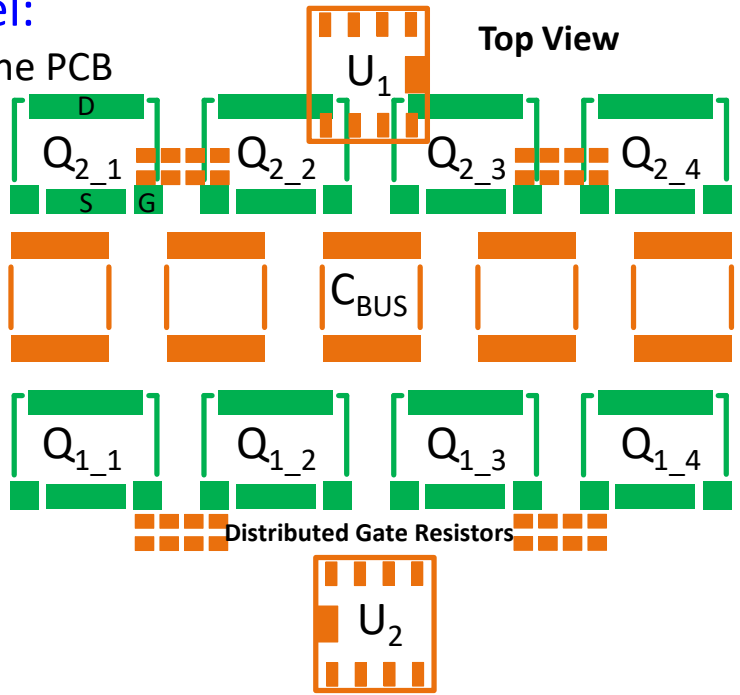
It is presented to show how the key components are placed on the PCB

- Low-side GaN gate driver design
- Same for high side GaN



Design rules of important loops

Important Loops	Components	Design Rule
Power Commutation Loop	$Q_{1\_1,2,3,4}$, $Q_{2\_1,2,3,4}$, C_{BUS}	1. As small as possible 2. Identical loop length for each paralleled device
Gate Driver Loop (turn-on)	R_{gon}, $R_{d1,3,5,7}$, $Q_{2\_1,2,3,4}$, $R_{d2,4,6,8}$, C_1, U_1	
Gate Driver Loop (turn-off)	R_{goff}, $R_{d1,3,5,7}$, $Q_{2\_1,2,3,4}$, $R_{d2,4,6,8}$, C_2, U_1	



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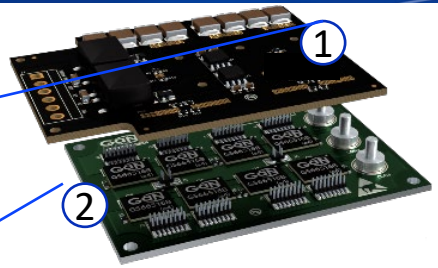
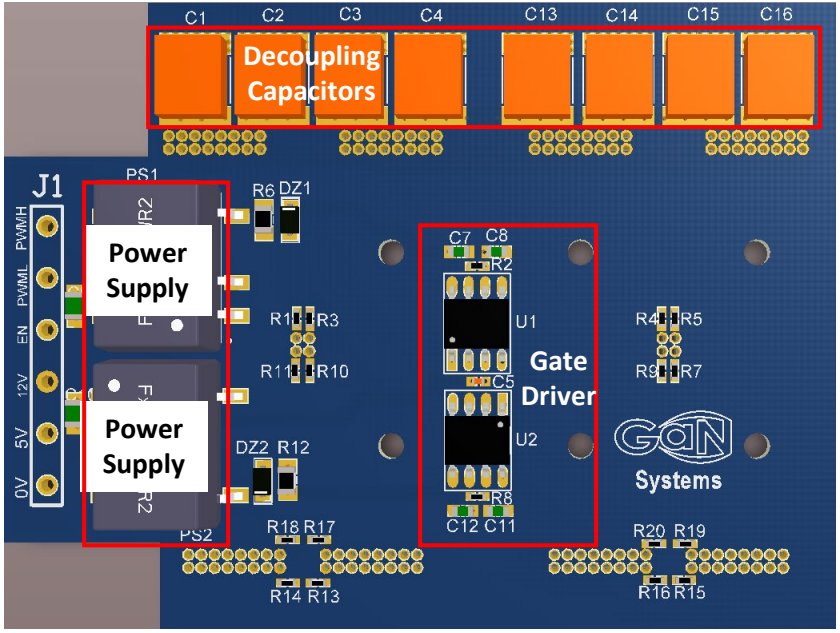
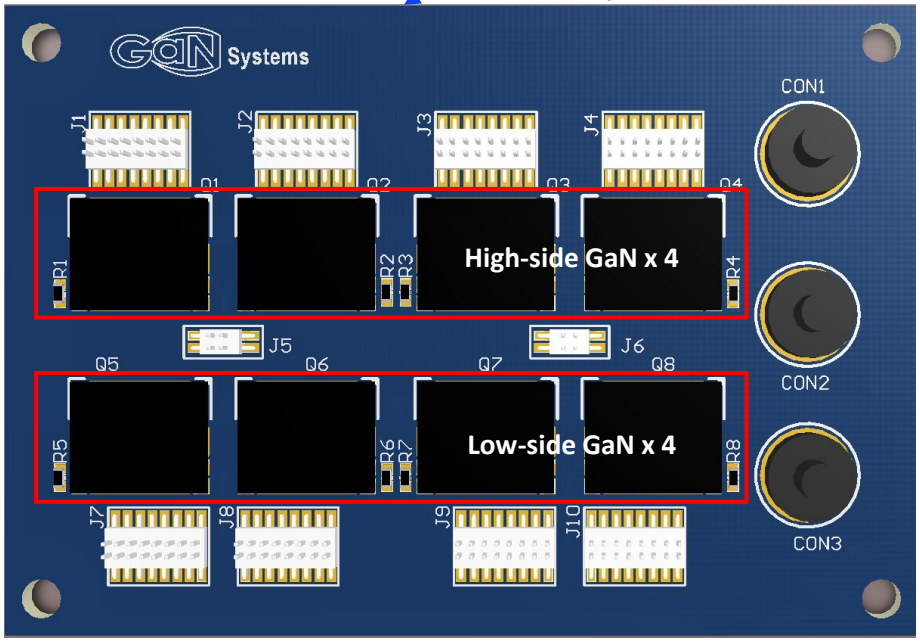
4 Real Example of **Paralleling 4xGS66516B**

- An example of **4x GS66516B in parallel** (650V 240A) IMS GaN module design is presented to illustrate how its gate driver and power stage layouts are designed





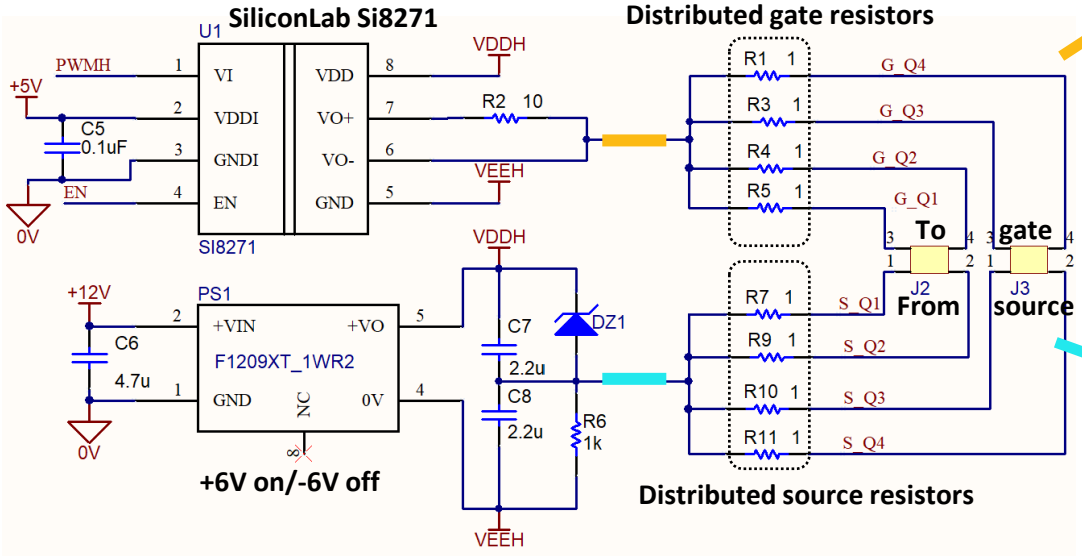
① **Gate Driver Board**



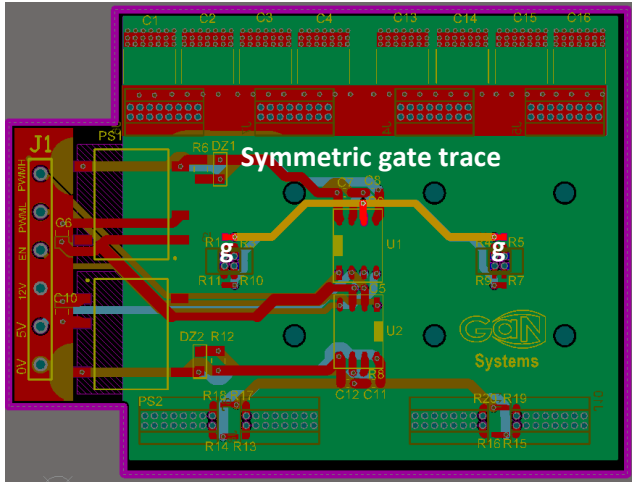
② **IMS Power Board**

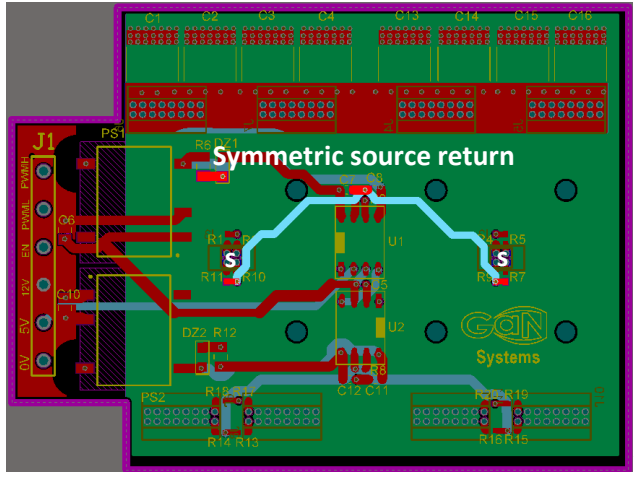
4 Paralleling 4xGS66516B: **Gate Driver Loop Layout Design**

- For gate driver loops, symmetric gate traces are observed



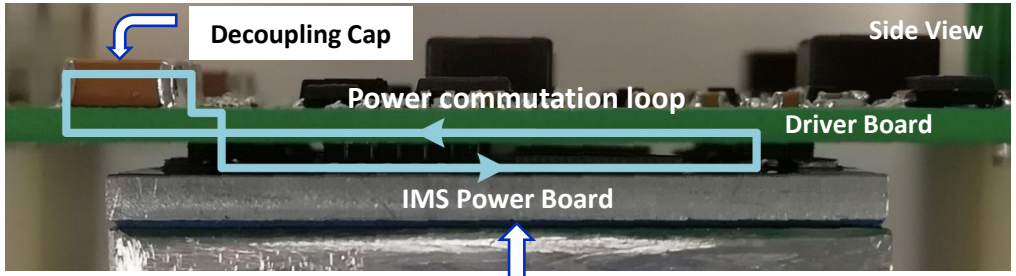
Schematic of Gate Driver Circuit

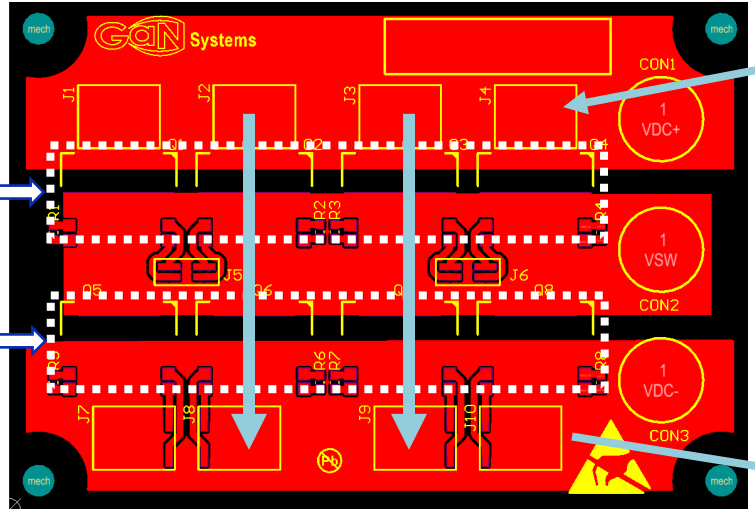




4 Paralleling 4xGS66516B: **Power Stage Layout Design**

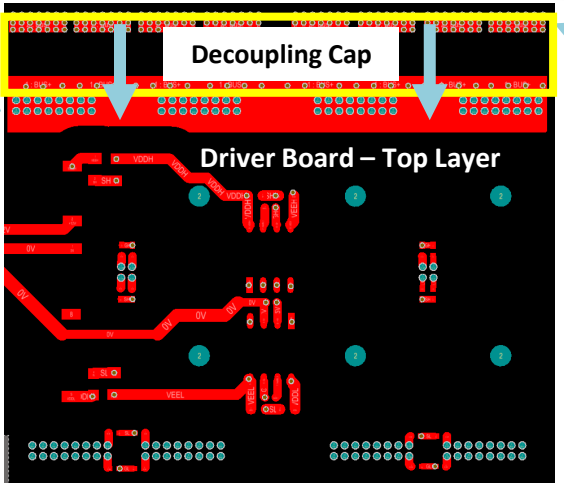
- Power commutation loop inductance is **effectively reduced** by flux cancellation

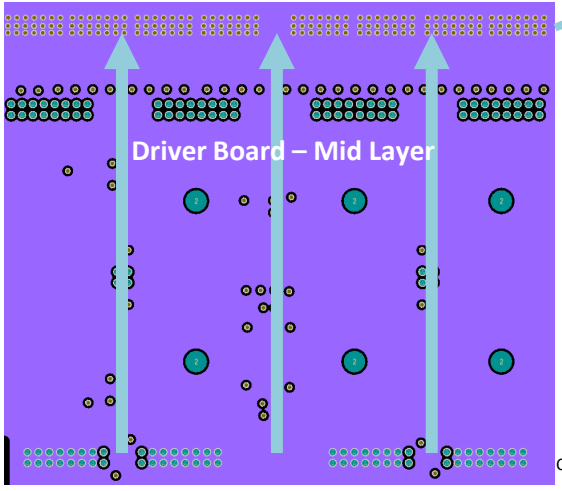




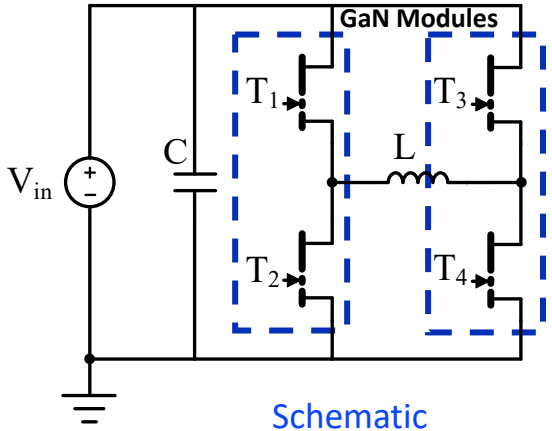
High-side GaN x4

Low-side GaN x4

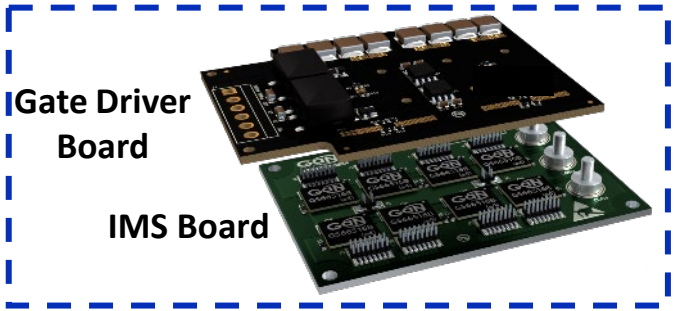




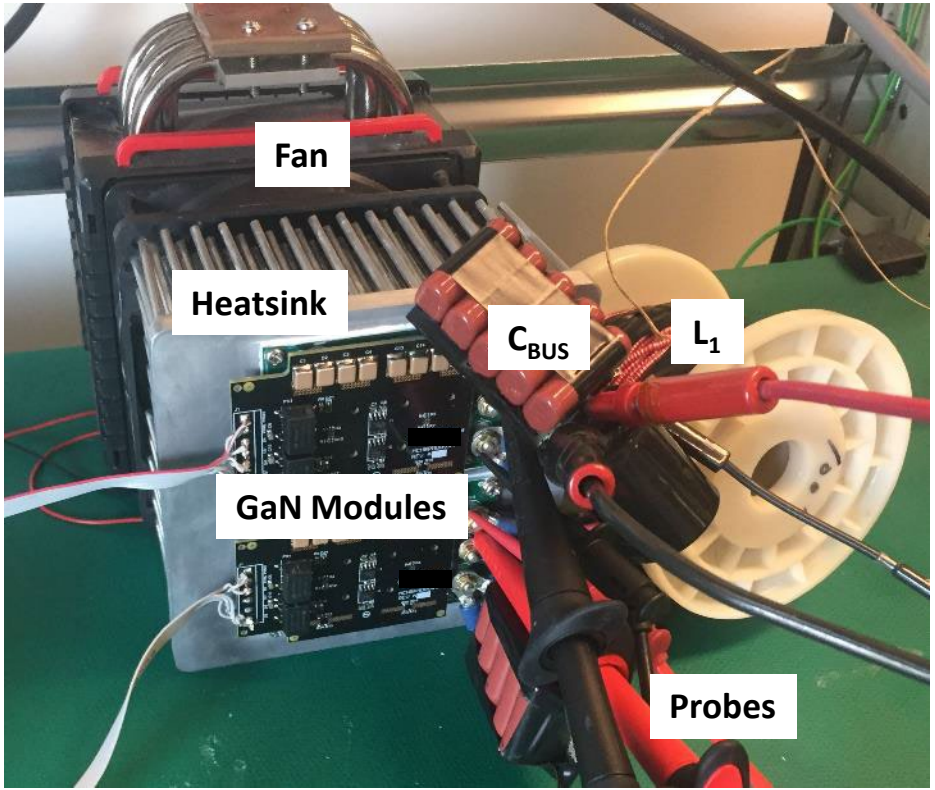
- A full power emulation test bench is built to test the 650V 240A GaN IMS module **under high power conditions**



Schematic

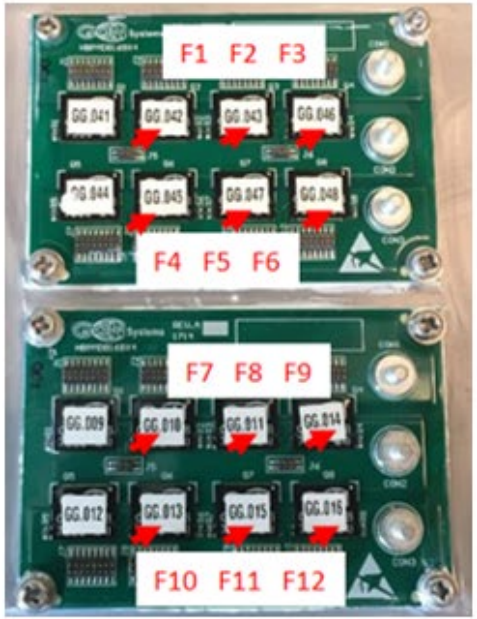


240A/650V Half bridge GaN module

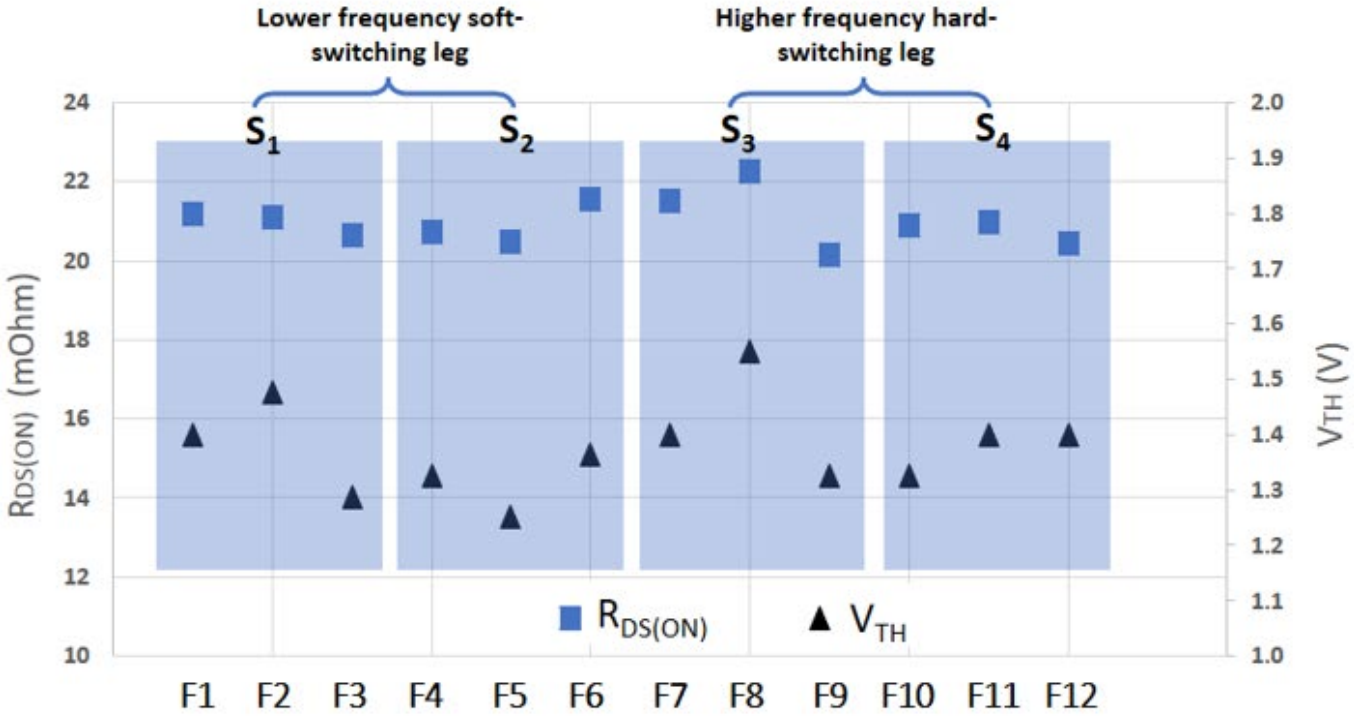


Experiment Bench

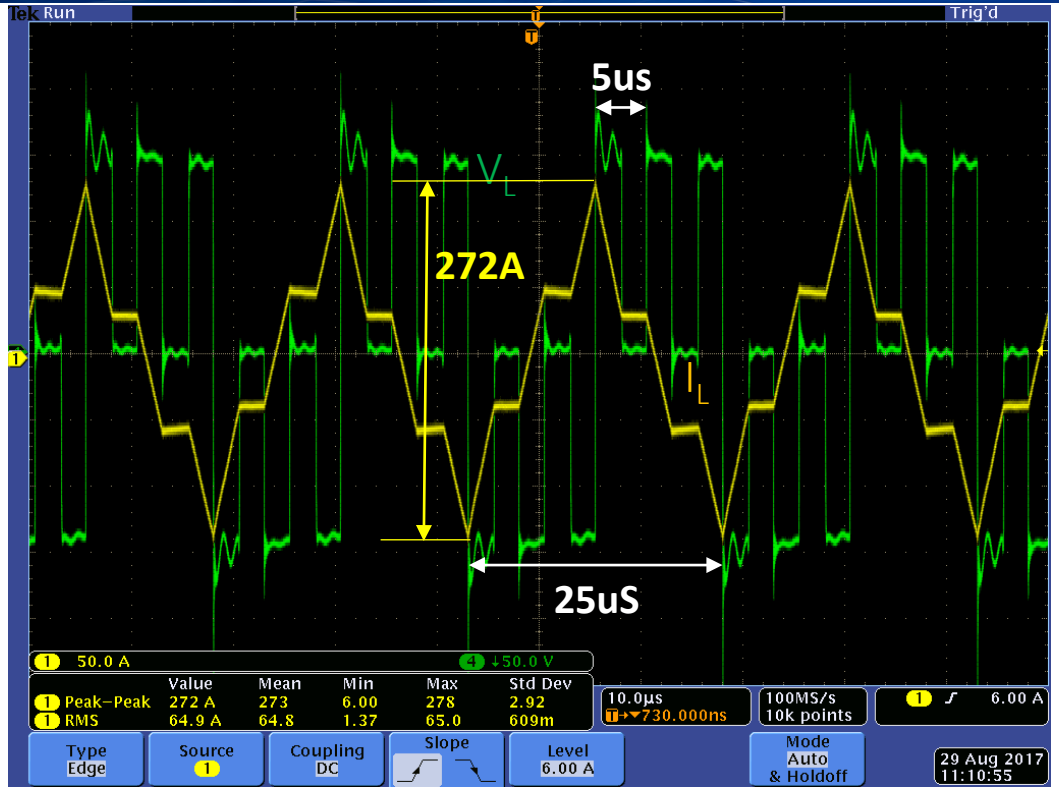
- GaN HEMTs **randomly** selected for paralleling



GaN power modules under test

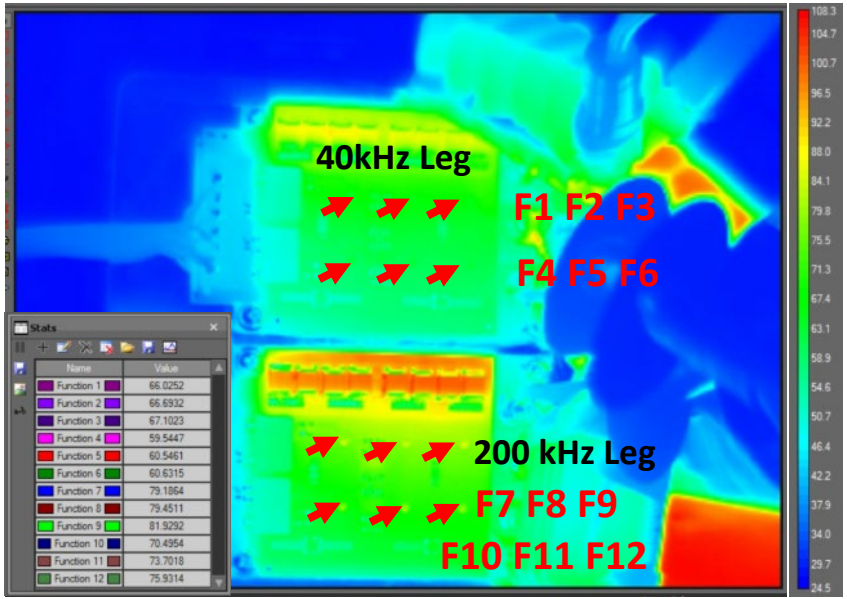


4 Paralleling 4xGS66516B: **Experimental Waveforms**

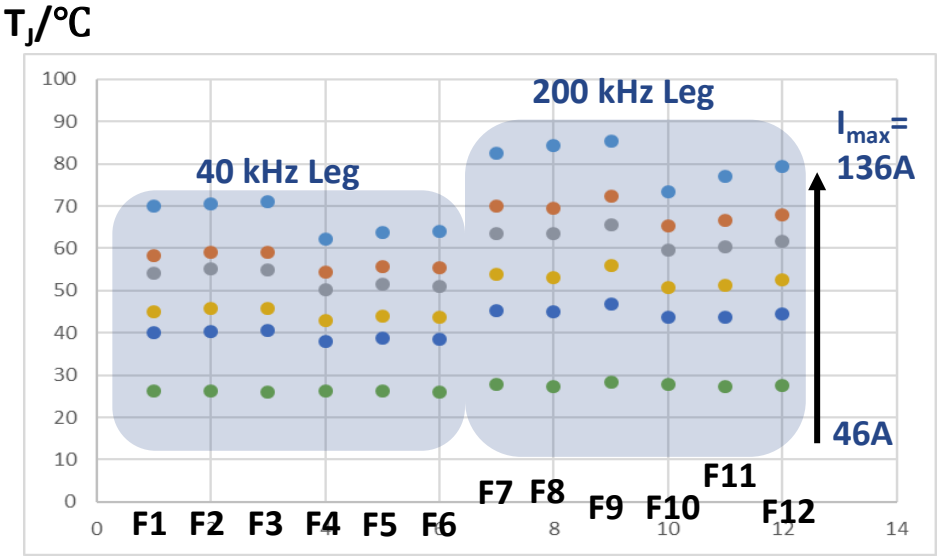


- Full power emulation test @ I_{max} = 136A, I_{RMS} = 65A, F_{SW} = 200kHz is performed
- Current and voltage switching waveforms are good

4 Paralleling 4xGS66516B: **Temperature Distribution**



Temperature Distribution@ I_{max}=136A



Temperature Distribution in All Operation Range

- Thermal **Balance is achieved** between un-pre-selected transistors – **no thermal runaway**
- **Good** thermal balance performance: the junction temperature difference is < 6℃ for the worst case, < 3℃ for the best case

Content

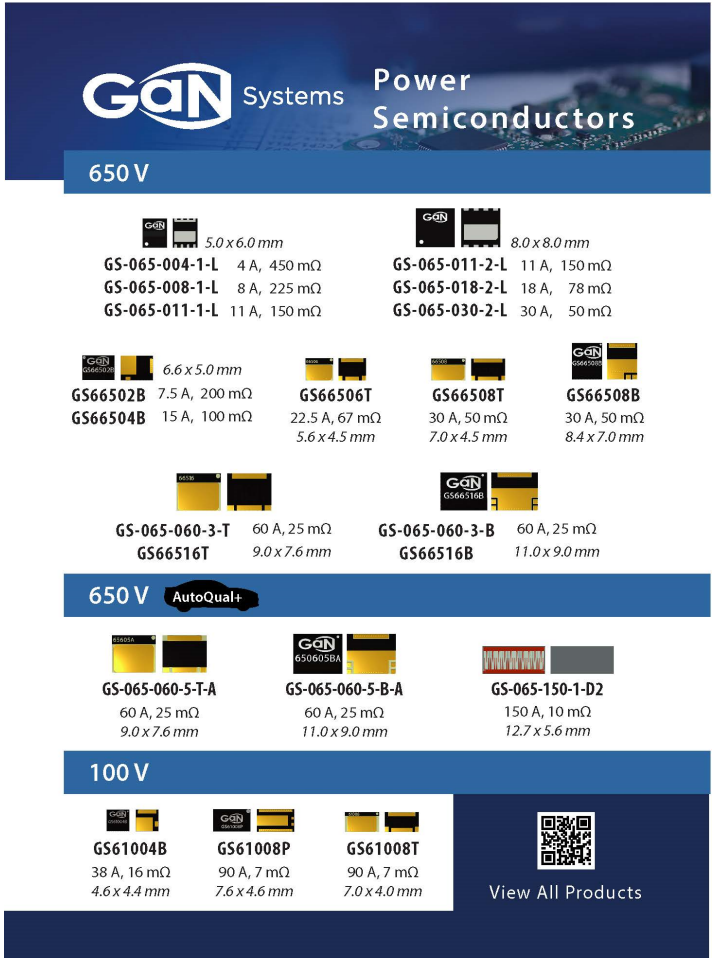
Summary

- GaN Systems E-HEMT device characteristics are **inherently fit for paralleling**:
  - **Positive** $R_{DS(on)}$ temperature coefficient
  - **Stable** gate threshold over the temperature range
  - **Negative transconductance** g_m temperature coefficient

- Layout is important for paralleling high speed GaN HEMT:
  - Low and balanced parasitic inductance on the power and gate drive loop
  - Equal length of gate drive layout and optimum gate driver circuit

- A design example of 4 x paralleled GaN HEMTs is presented and the test results show that the **thermal balance of GaN HEMTs is achieved**

Product Portfolio



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