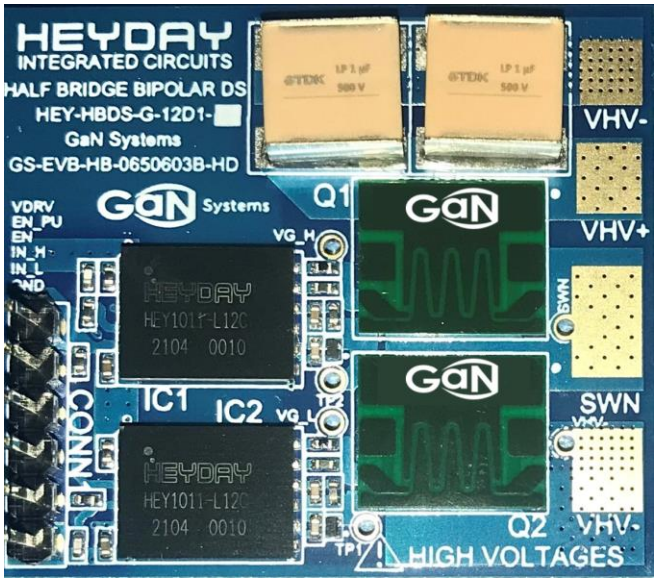
GS-EVB-HB-0650603B-HD

Half Bridge Bipolar Drive Switch Board

Technical Manual



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DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Please sure that appropriate safety procedures are followed. This evaluation kit is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY**. Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. **There is NO built-in electrical or thermal protection on this evaluation kit**. The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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1 Overview

1.1 Introduction

The Integrated Circuits Half Bridge Driver-Switch GS-EVB-HB-0650603B-HD is a demonstration board containing two HEY1011-L12C GaN FET drivers and two 650V, 60A GaN FETs configured in a half bridge configuration.

The datasheet for the HEY1011-L12C in this board can be found here.

The GS-EVB-HB-0650603B-HD can be used to perform double pulse tests, or to interface the half bridge to an existing LC power section, both as shown below.

The isolated HEY1011-L12C driver does not require secondary side power or bootstrap components. Gate drive power is supplied to secondary side from the primary side supply voltage V_{DRV}. The amplitude of the gate drive can be varied by varying V_{DRV} between 7 V and 15 V.

1.2 Quick Start Guide

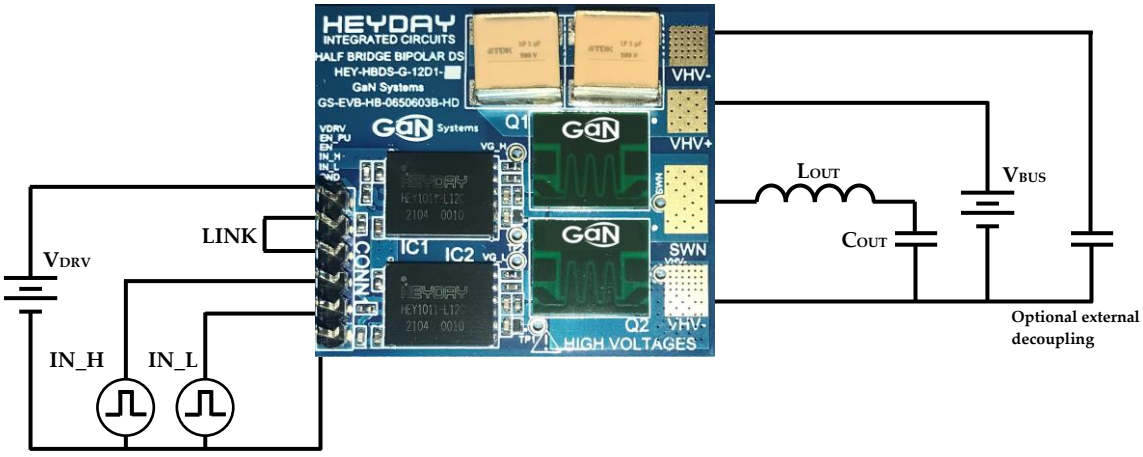

Figure 1: GS-EVB-HB-0650603B-HD Quick Start

1. Apply V_{DRV} = 12V
2. Link pins EN_PU and EN (if not using external Enable control)
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points a located on the test board as shown above. A suitable differential oscilloscope should be used to monitor the high side gate signal from V_{GH} to V_{SW}.

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2 Technical Description

2.1 Gate Pull Up and Pull Down Resistors

The HEY1011-L12C gate driver has independent output pins for the gate pull up and gate pull down allowing control of the turn-on and turn-off rise and fall times.
The default values for these resistors are:

- OUTPU: R1 and R5 = 10 Ohms
- OUTPD: R3 and R7 = 1 Ohm

These values can be modified to suit your own application.

2.2 Enable and Start Sequence

The HEY1011-L12C has an open drain enable pin (EN) to facilitate a system level wired-AND start up.

When the enable pin is externally pulled low this forces the driver into a low power mode. The driver output is pulled low in this mode. In the event of an internal fault condition, such as UVLO, this pin is actively pulled low internally by the driver. During normal operation, the pin is released by the driver, and must be pulled high with an external pull-high resistor. This functionality can be used by the PWM controller as an indication that it can start sending IN pulses to the driver. It is typically wired AND with the controller enable pin as shown in Figure 2 below.

The GS-EVB-HB-0650603B-HD evaluation board provides direct access to the EN pin on connector CONN1. Internally the board contains a 100k pull up resistor connected from VDRV to the EN_PU pin on connector CONN1 – see schematic in Figure 11. If external control of the enable function is not required, pins EN and EN_PU must be linked together on CONN1 to make use of the internal 100k pull up resistor to enable the driver. If the EN pin is left floating, the drivers will not respond to INL or INH input signals.

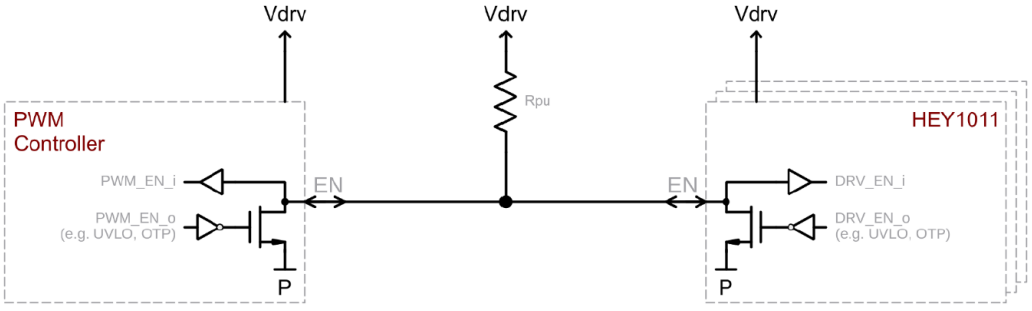

Figure 2: HEY1011-L12C Wired-AND enable

The start up sequence of the HEY1011-L12C is shown in Figure 3 below. Time T_{START} is defined as the time after which V_{DRV} reaches the UVLO rising level to the HEY1011-L12C releasing the EN internal pull down.

IMPORTANT the IN signal must not be applied before the EN pin has been released.

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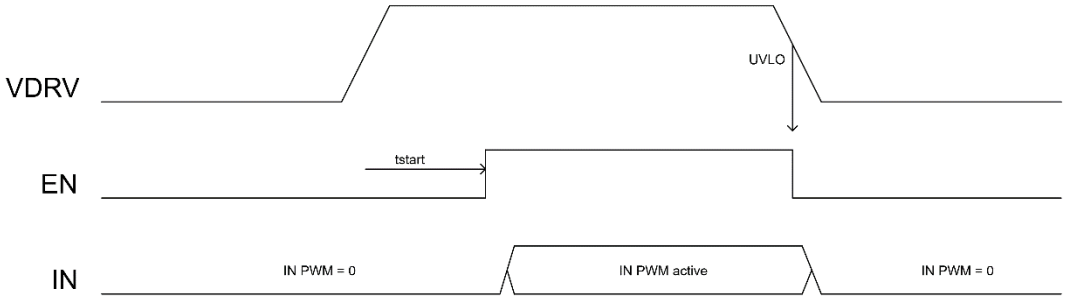

Figure 3: HEY1011-L12C Start up sequence.

2.3 Measurement Points

The GS-EVB-HB-0650603B-HD EVB contains convenient test points for monitoring the high and low side gate drives as well as the switch node as shown in Figure 4 below.

When measuring V_{GS_H} use a differential probe with suitable ratings for the applied bus voltage. The GS-EVB-HB-0650603B-HD EVB uses a bipolar gate drive arrangement as shown in Figure 5 below. When measuring V_{GS}, both gate drives are measured relative to the source of their associated GaN FET. Therefore, the off-state voltage will be negative.

It is important to use a low inductance scope probe ground lead as shown to avoid pickup of spurious switching noise.

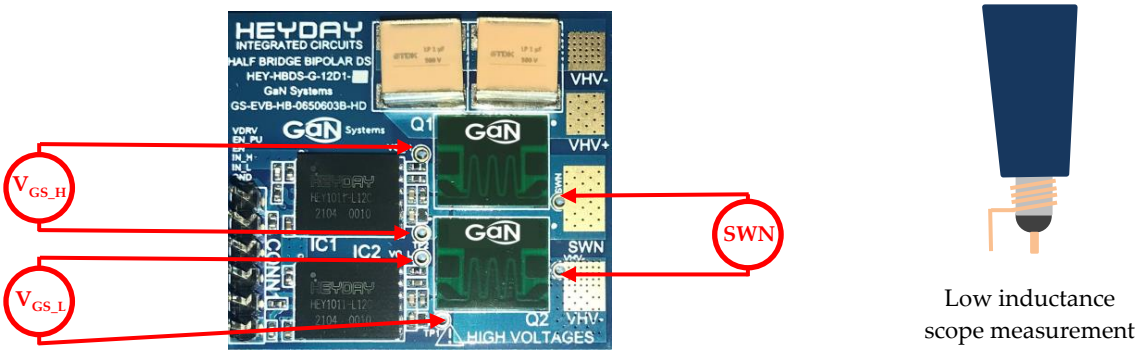

Figure 4: Measurements points

2.4 Bipolar Gate Drive

Due to the high rate of change of voltages and currents in power switching circuits, unwanted inductor currents and capacitor voltage drops can be created.

One such example is the false turn on of a FET due to a dv/dt event. In a half bridge circuit, after the low side FET has been turned off and a suitable dead-time elapsed, the high side FET is turned on. This produces a rapidly changing switch node voltage at the drain of the low side FET. This voltage will produce a capacitor current:

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$$i_{C_{GD}} = C_{GD} \frac{dV_{DS\_L}}{dt}$$

flowing in the gate-drain capacitance, C_{GD}, and driver output. It will cause the voltage on the gate of the low side FET to rise. If this voltage spike peaks beyond the threshold voltage V_{TH}, the FET will conduct. Considering that the high side FET is also conducting, this can result in a potentially destructive shoot-through event.

The GS-EVB-HB-0650603B-HD EVB uses a bipolar gate drive arrangement which is useful to mitigate against the effects of gate-drain capacitor currents. The secondary supply voltage V_{SEC} is a function of the primary supply voltage V_{DRV}. The zener diode, CR1, will regulate the positive turn on voltage of the GaN FET. During the turn-off of period, the gate voltage will be negative with a value of:

$V_{GS\_OFF} = V_{SEC} – V_{ZENER}$. V_{SEC} is typically 9 V.

This negative V_{GS_OFF} voltage allows more margin before the threshold voltage can be reached.

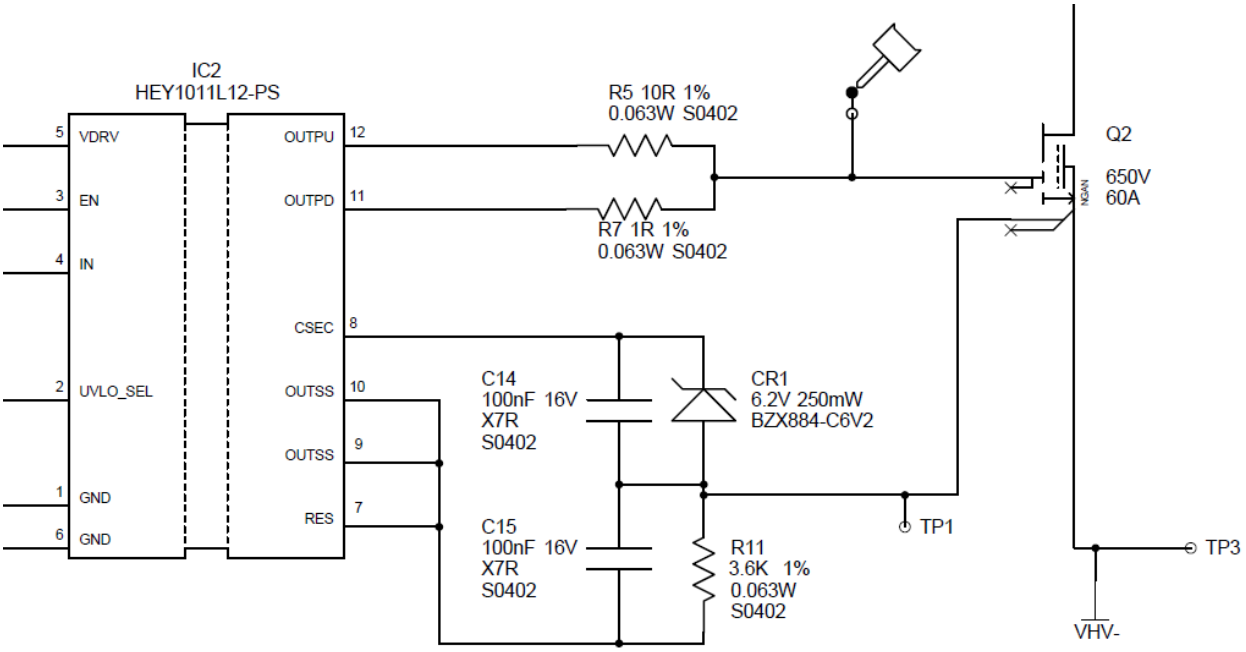

Figure 5: Bi-polar gate drive schematic

2.5 Propagation Delay

- V_{DRV} = 12V
- Input = 100kHz
- R_{PU} = 10R, R_{PD} = 1R
- Power train un-loaded. That is, VHV+ = 0V.

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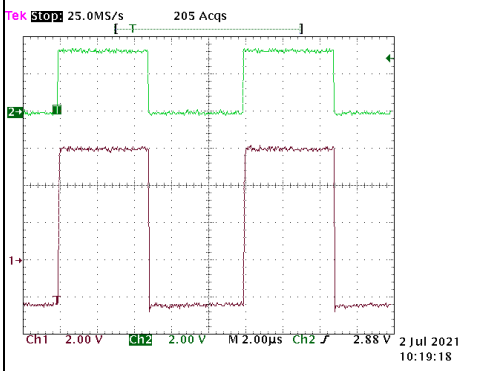	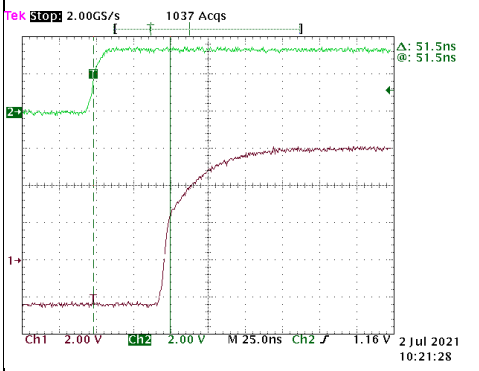	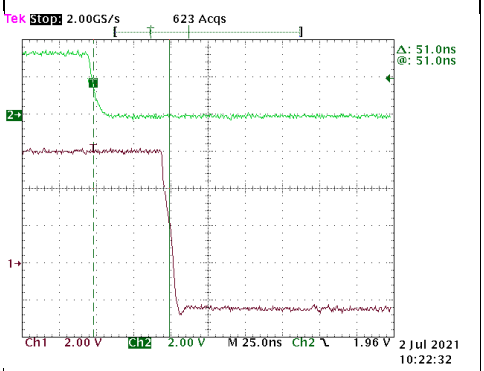
CH2: Low side driver input **CH1:** Low side driver (IC2) output wrt VHV-	**CH2:** Low side driver input **CH1:** Low side driver (IC2) output wrt VHV-	**CH2:** Low side driver input **CH1:** Low side driver (IC2) output wrt VHV-
Low side driver output	**Typical Turn-on Propagation Delay**	**Typical Turn-off Propagation Delay**

Figure 6: Typical Driver output at 100kHz

3 Test results

3.1 Double pulse test

The double pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.

For a low side switch the setup is as shown below:

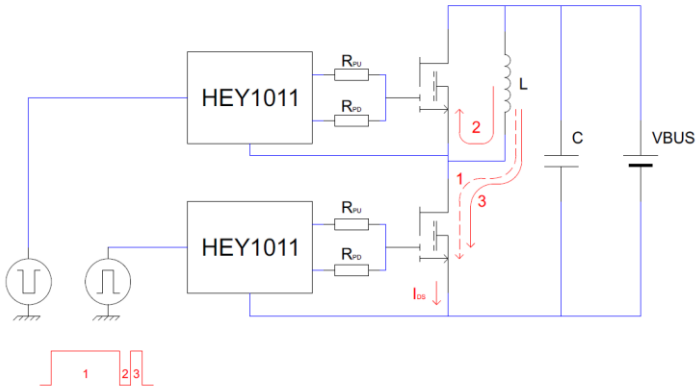

Figure 7: Double Pulse Test

The low side switch is driven with two pulses as shown below. The high side switch can be held off or driven with the inverse of the low side gate switch (with adequate dead time).

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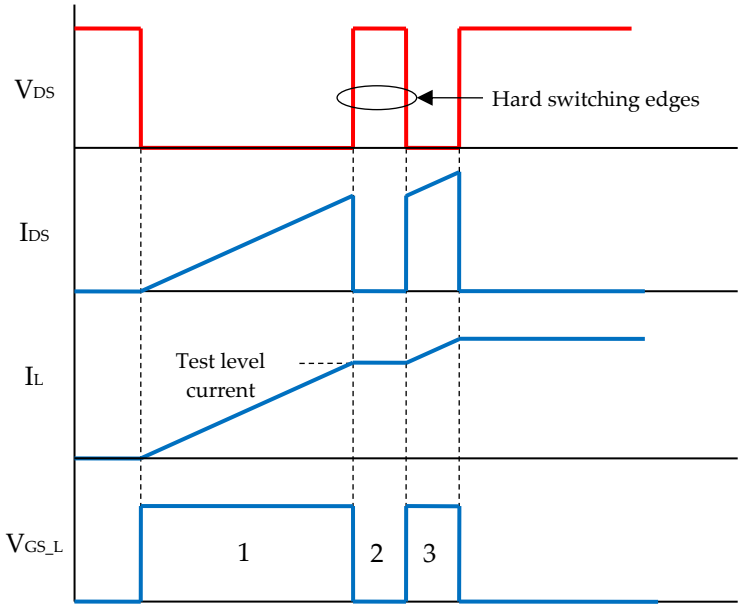

Figure 8: Double Pulse Test Waveforms

An inductor is placed in parallel with the high side switch. The goal of this inductor is to establish the test level current in the low side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = \frac{V_{BUS}\, T_{ON\_1}}{L}$$

During period 2, the inductor current will naturally decay. The duration of period 2 should not be too long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current will again rise. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

3.2 Components Specification

	COMPONENTS
Drivers:	Heyday HEY1011-L12C
Inductor:	49uH 360mΩ Air Core
R_{PU}:	10Ω
R_{PD}:	1Ω

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3.3 DPT Result 100V – 15A

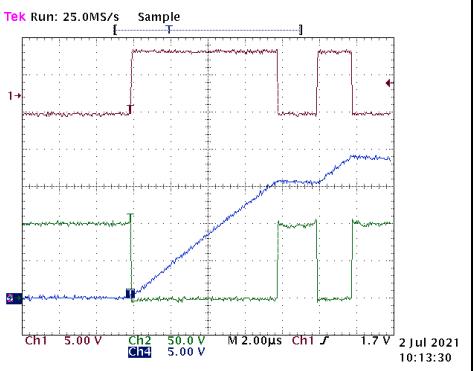	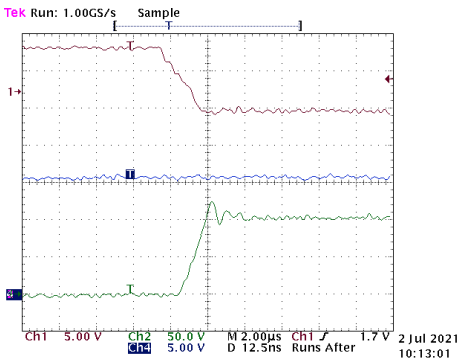	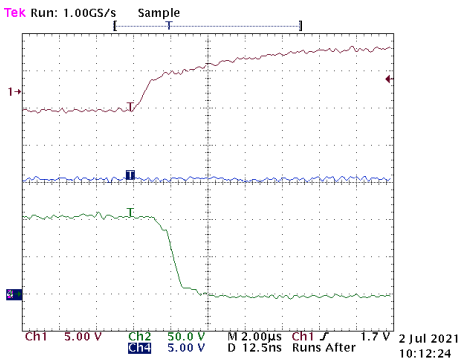
CH1 (Red): Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current (1A/V)	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**
DPT Overview	**DPT Hard switching turn off**	**DPT Hard switching turn on** **Time base (12.5ns/div)**

Figure 9: DPT 100V – 15A

3.4 DPT Result 400V – 62A

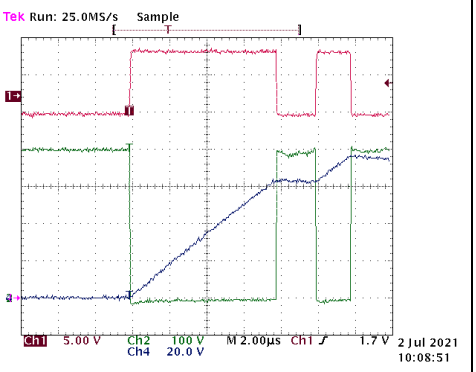	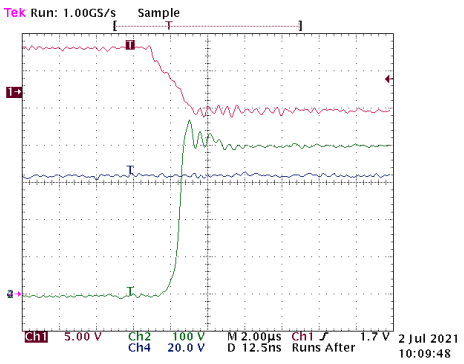	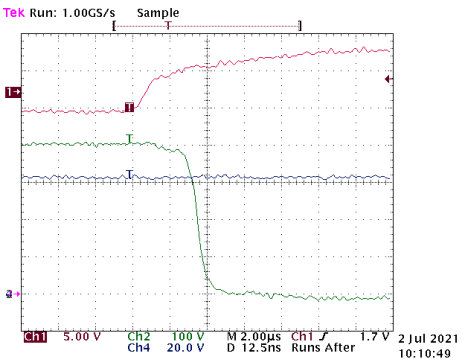
CH1 (Red): Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current (1A/V)	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**
DPT Overview	**DPT Hard switching turn off**	**DPT Hard switching turn on** **Time base (12.5ns/div)**

Figure 10: DPT 400V – 62A

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4 Schematic

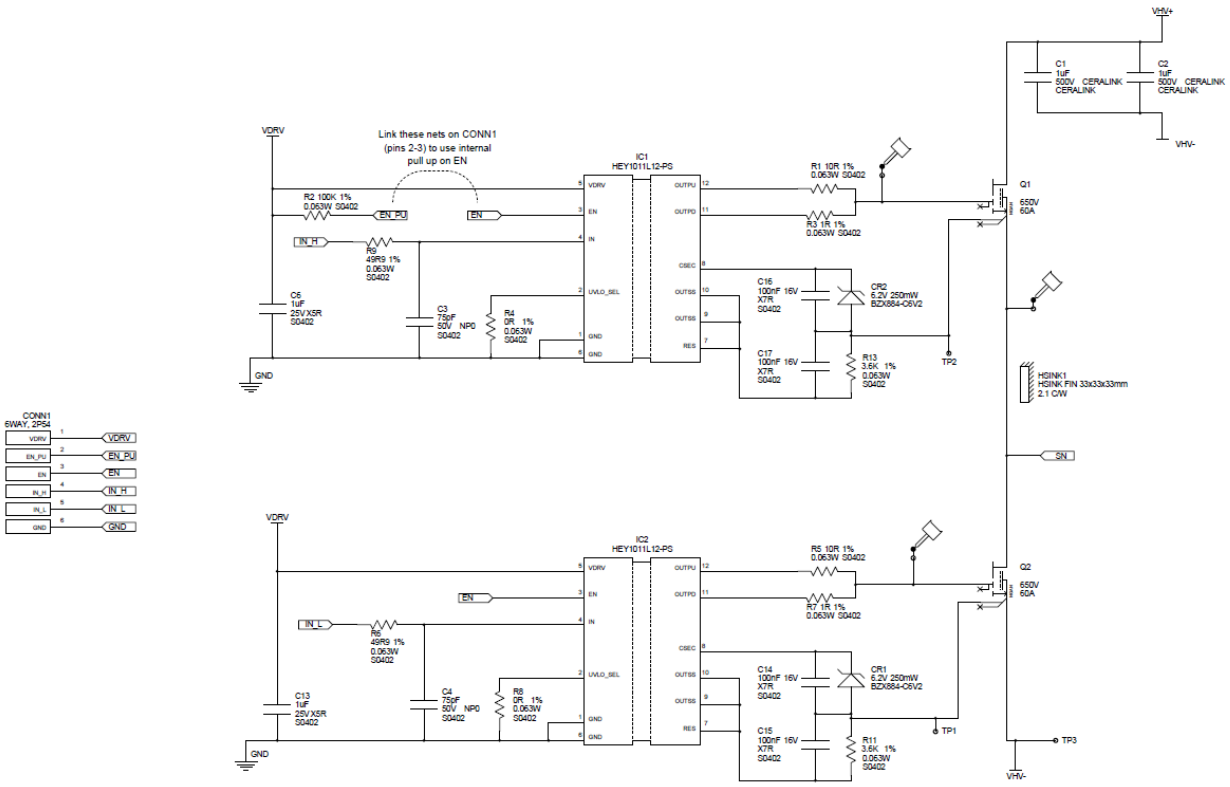

Figure 11: GS-EVB-HB-0650603B-HD Schematic

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5 Layout

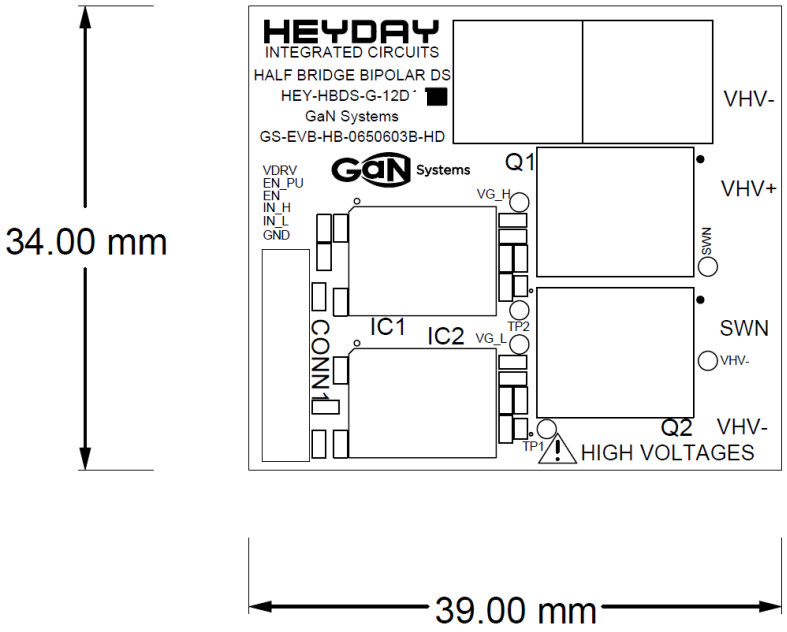

Figure 12: GS-EVB-HB-0650603B-HD Silkscreen and component placement

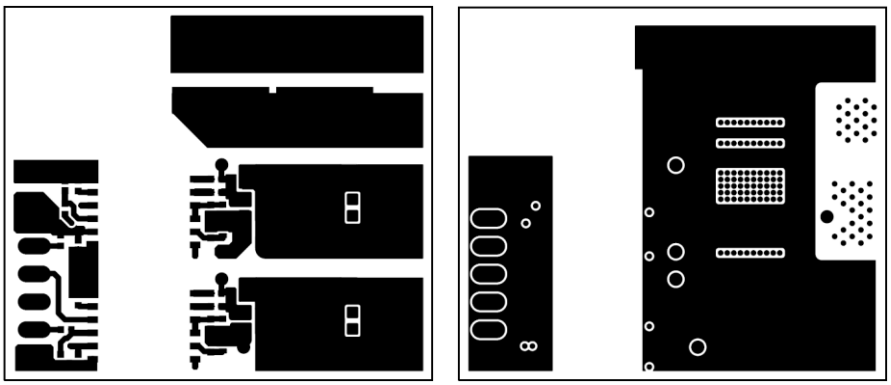

Figure 13: GS-EVB-HB-0650603B-HD Top Side Copper (L) and Layer 2 Copper (R)

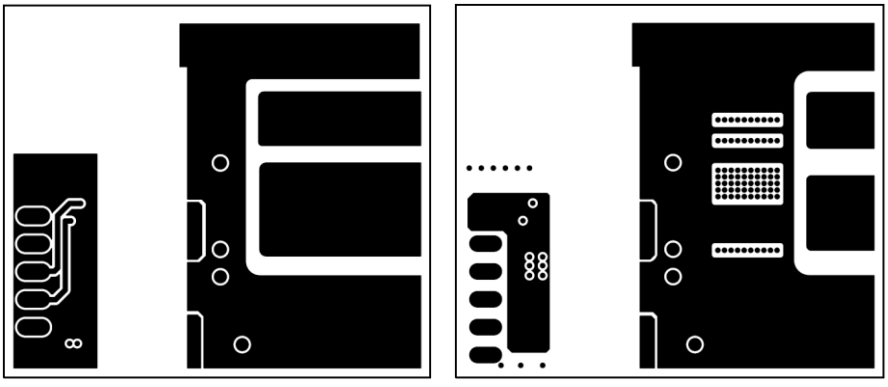

Figure 14: GS-EVB-HB-0650603B-HD Layer 3 Copper(L) and Bottom Side Copper (R)

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6 Bill of Materials

Table 1: Bill of materials

Item	Ref Name	Description	Value	Qty	Manufacturer	Manufacturer PN
1	C1, C2	CAP CERALINK, 1uF,500V PLZT	1uF	2	TDK	B58031U5105M062
2	C14,C15,C16,C17	CAP, CER,100nF,16V,X7R, S0402	100nF	4	KEMET	C0402C104K4RALTU
3	C3,C4	CAP, CER, 75pF,50V,NP0, S0402	75pF	2	KEMET	C0402C750J5GACTU
4	C6,C13	CAP, CER,1uF,25V,X5R, S0402	1uF	2	MURATA	GRM155R61E105KA12D
3	CONN1	HEADER, 6 WAY, 2.54mm	6WAY, 2P54	1	WURTH	61300611121
6	CR1,CR2	DIO ZEN, 6V2, 250mW, 2%, SOD882	BZX884-C6V2	2	NEXPERIA	BZX884-B6V2,315
7	IC1,IC2	GaN FET Driver	HEY1011-L12C	2	HEYDAY IC	HEY1011-L12C
8	Q1,Q2	NGAN 650V 60A	NGAN 650V 60A	2	GAN SYSTEMS	NGAN 650V 60A
9	R1,R5	RES, SMD, 10R, 0.063W, 1%, S0402	10R	2	VISHAY	CRCW040210R0FKED
10	R11,R13	RES, SMD, 3K6, 0.063W, 1%, S0402	3.6K	2	PANASONIC	ERJ2RKF3601X
11	R2	RES, SMD, 100K, 0.063W, 1%, S0402	100K	1	PANASONIC	ERJ2GEJ104X
12	R3,R7	RES, SMD, 1R0, 0.063W, 1%, S0402	1R	2	VISHAY	CRCW04021R00FKED
13	R4,R8	RES, SMD, 0R0, 0.063W, 1%, S0402	0R	2	VISHAY	RCG04020000Z0ED
14	R6,R9	RES, SMD, 49R9, 0.063W, 1%, S0402	49R9	2	VISHAY	CRCW040249R9FKED

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