Self-Powered Single-Channel Isolated GaN FET Driver With *Power-Thru™* Integrated Isolated Bias Supply

1. Features

- ***Power-Thru™*** integrated isolated bias
  - No high-side bootstrap
  - No external secondary-side bias
- 50-ns propagation delay, with excellent device-to-device matching of 5 ns
- Separate drive output pins pull-up (2.8 Ω) and pull-down (1.0 Ω)
- Wide supply voltage 7.5 V < V_{DRV} < 15 V
- UVLO on primary V_{DRV} and secondary V_{SEC}
- EN enable pin with fast response
- Continuous ON capability – no need to recycle IN or recharge bootstrap capacitor
- CMTI > 100 V/ns dv/dt immunity
- Creepage distance > 8 mm
- Distance-through-insulation DTI ≥ 450 µm
- Safety Regulatory Approvals (pending)
  - 5.7 kV RMS V_{ISO} per UL 1577
  - 8 kV pk V_{IOTM} maximum transient isolation voltage per VDE0884-11
  - 630 V pk maximum working isolation voltage

2. Applications

- **AC-DC and DC-DC converters** – Totem-pole PFC, Half-/Full-Bridge, LLC, SR Drive, Multi-level converters, Phase-Shifted Full-Bridge, etc.
- **Automotive** – EV chargers, motor drives
- **Industrial** – transportation, robotics
- **Grid Infrastructure** – micro-inverters, solar

3. General Description

The HEY1011 isolated gate driver is optimised for driving GaNFETs in multiple applications and topologies. An isolated output bias supply is integrated into the driver device, eliminating the need for any external gate drive auxiliary bias supply or high-side bootstrap. This greatly simplifies the system design and reduces EMI through reduced total common-mode (CM) capacitance. It also allows the driving of a floating switch in any location in a switching power topology.

The driver has fast propagation delay and high peak source/sink capability to efficiently drive GanFETs in high-frequency designs. High CMTI combined with isolated outputs for both bias power and drive make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity.

The device is available in a compact low-profile surface-mount LGA package. Several protection features are integrated, including UVLO on primary and secondary bias rails, internal pull-down on IN pin and OUTPD pin, fast-response enable input, and OUT pulse sychronisation with first IN rising edge after enable (avoids asynchronous runt pulses).

Figure 1: LGA: 10 x 7.66 x 1.91mm 12-pin integrated package

3.1. Typical Application Diagram

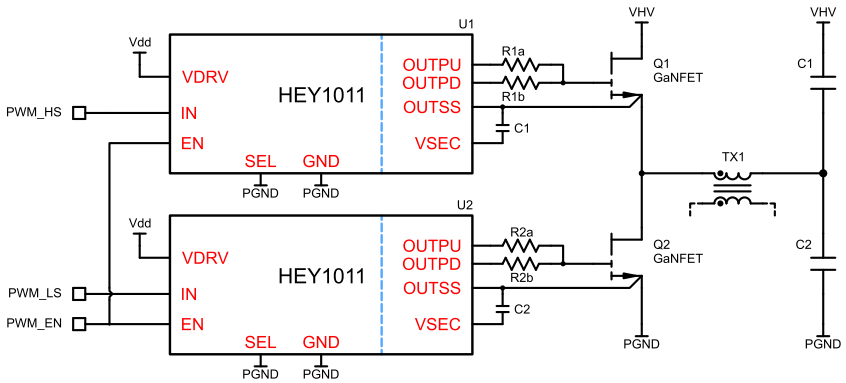


Figure 2: Typical HEY1011 Half-bridge application – eliminates high-side bootstrap

4. Contents

5. Typical applications

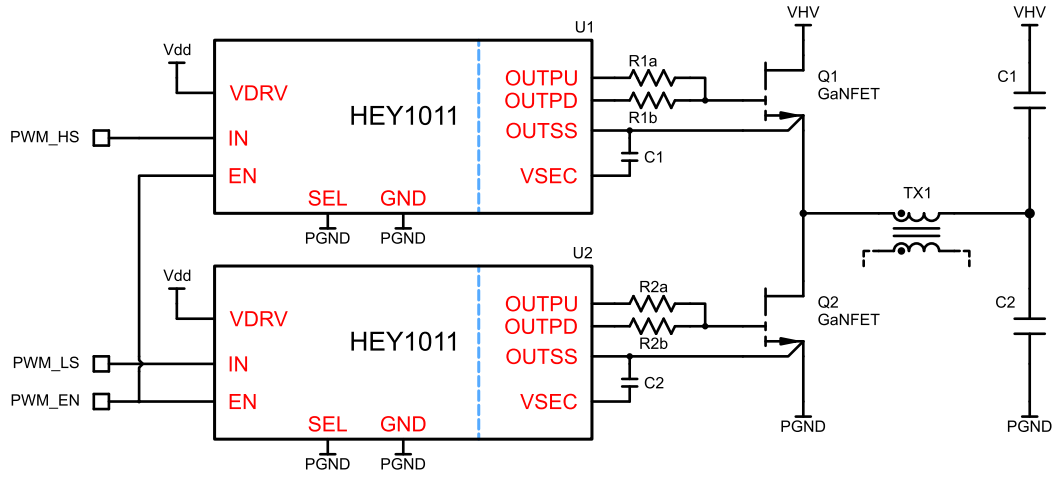


Figure 3: Half-Bridge with HEY1011 as high and low side drivers

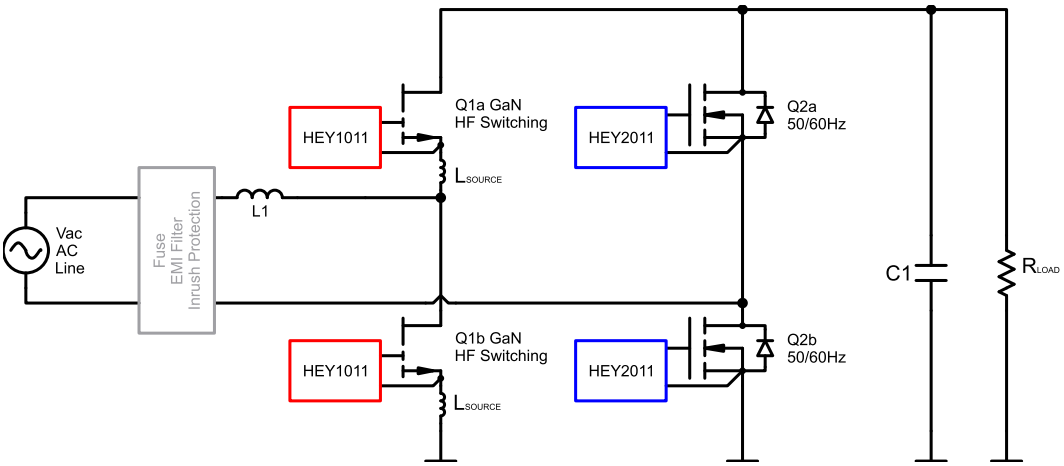


Figure 4: Totem pole PFC: HEY1011 (GaN version) and HEY2011 (MOS version) as high and low side drivers

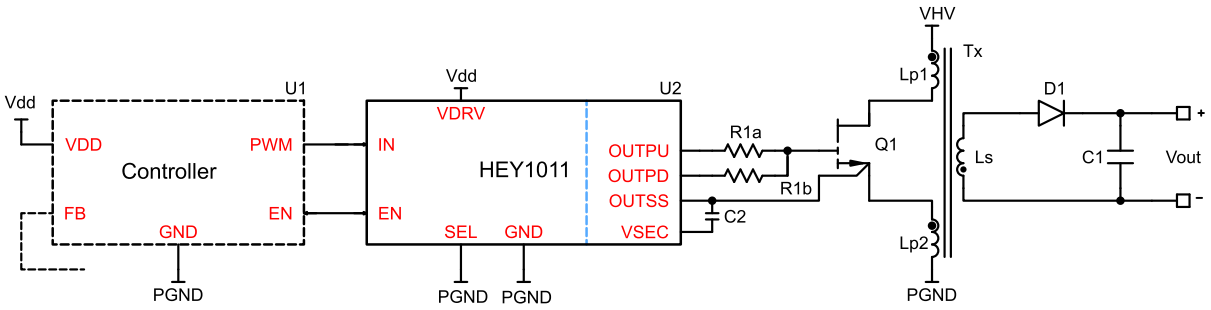


Figure 5: Centre switched Flyback – HEY1011 driving centre tapped switch (symmetrical bipolar voltage swings)

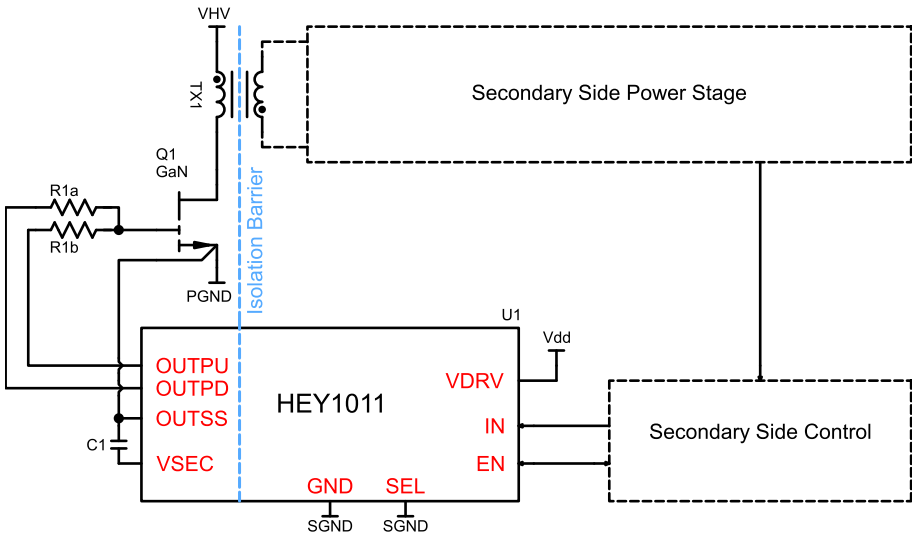


Figure 6: Secondary control to primary drive - Hey1011 single driver

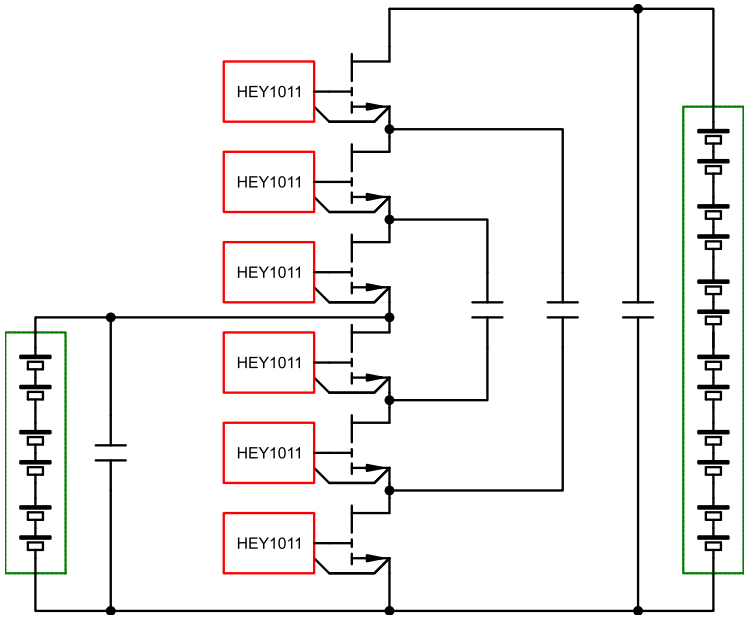


Figure 7: Multi-Level Converter – stacked low voltage switches results in higher efficiency. Hey1011 makes this easy to drive.

6. Internal Block Diagram

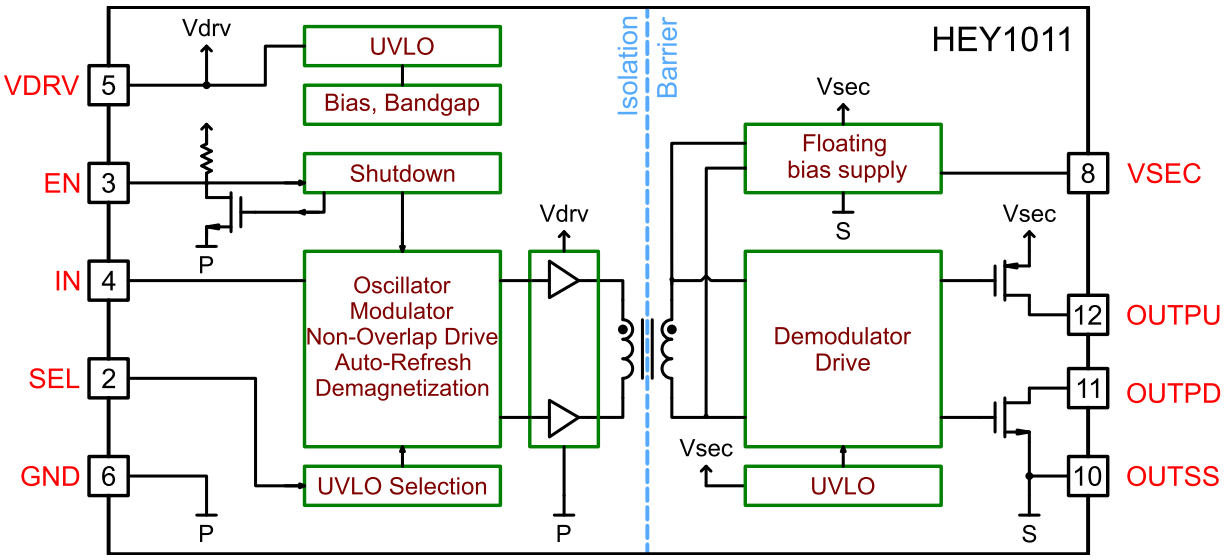


Figure 8: HEY1011 Block Diagram

7. Pin Descriptions

Pin Number	Pin Name	Pin Function
1	GND	Internally connected to GND; recommend external connection to GND net (pin 6) to improve thermal impedance; can be left floating if necessary.
2	SEL	Selects the UVLO voltage. See section 9.1 HEY1011 UVLO selection
3	EN	Bidirectional enable pin. Figure 9
4	IN	PWM input. Table 7
5	VDRV	Ground referenced voltage supply. This voltage indirectly sets the output gate drive amplitude.
6	GND	Ground pin for input/primary side
7	OUTSS	Internally connected to OUTSS; recommend external connection to OUTSS net (pins 9, 10) to improve thermal impedance; can be left floating if necessary. See section 9.6
8	VSEC	External capacitor referenced to OUTSS.
9	OUTSS	Isolated output return pin
10	OUTSS	Isolated output return pin
11	OUTPD	Isolated output drive pull-down pin. Table 7
12	OUTPU	Isolated output drive pull-up pin. Table 7

Table 1: HEY1011 pin descriptions

8. Specifications

8.1. Absolute Maximum Ratings(1)

Symbol	Parameter	Min	Max	Unit
VDRV	Drive supply voltage VDRV to GND	GND - 0.5V	17	V
IN	Input data, IN to GND	GND - 0.5V	17	V
EN	Enable, EN to GND	GND - 0.5V	17	V
SEL	UVLO voltage selection, SEL to GND	GND - 0.5V	3.6	V
OUTPU	Output drive pull up, OUTPU to OUTSS	OUTSS - 0.5V	17	V
OUTPD	Output drive pull down, OUTPU to OUTSS	OUTSS - 0.5V	17	V
VSEC	Isolated bias supply, VSEC to OUTSS	OUTSS - 0.5V	17	V
Tj	Junction Temperature	-40	150	°C

1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Table 2: Absolute maximum ratings

8.2. ESD Ratings

Electrostatic Discharge		Value	Unit
V_{ESD}	Human body model (HBM)	± 2	kV
	Charge Device Model (CDM)	± 500	V

Table 3: ESD ratings

8.3. Thermal Information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	tbd	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	tbd	°C/W

Table 4: Thermal Information

8.4. Recommended Operating Conditions

-40°C < T_J < 125°C, 7.5 V < V_{DRV} < 15 V, C_{sec} = 22 nF, C_{out} = 1 nF. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage Pins						
V_{DRV}	Drive supply voltage	See Table 10	7.5		15	V
Input Pins						
IN	Input Data		GND		V_{DRV}	V
EN	Enable Active High		GND		V_{DRV}	V
SEL	UVLO voltage selection pin		GND		3.3	V
Output Pins						
OUTPU	Output pull-up		0		15	V
OUTPD	Output pull-down		0		15	V
VSEC	Isolated supply referenced to OUTSS		0		15	V
T_J	Junction Temperature		-40		125	°C

Table 5: Recommended Operating Conditions

8.5. VSEC Pin Capacitor

-40°C <T_J< 125°C, 7.5 V < V_{DRV} < 15 V, C_{sec} = 22 nF, C_{out} = 1 nF. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VSEC pin capacitor C_{SEC}						
C_{SEC}	External capacitance connected between VSEC and OUTSS pins	External C_{OUT} = 1 nF	5 (1)	27	100 (2)	nF

1. *Smaller C_{SEC} values than the recommended typical value can give higher voltage ripple on CSEC*
2. *Larger C_{SEC} values will mean longer start up times.*

Table 6: Recommended C_{SEC} capacitor value

8.6. Electrical Characteristics

-40°C < T_J < 125°C, 7.5 V < V_{DRV} < 15 V, C_{sec} = 22 nF, C_{out} = 1 nF. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Currents						
I_{DRV_Q}	V_{DRV} quiescent current	IN=0, V_{DRV} = 12 V		2		mA
I_{DRV_SW}	V_{DRV} switching current	F_S = 100 kHz, V_{DRV} = 12 V		4.2		mA
Input Pins						
IN	Input Data	Logic low			1.0	V
		Logic High	2.0			
	Hysteresis			300		mV
EN	Enable Active High	Logic low			1.0	V
		Logic High	2.0			
	Hysteresis			400		mV
R_{IN}	IN pin input pull down resistance on chip			300		kΩ
Output Pins						
R_{PU}	OUTPU pull up resistance			2.8		Ω
R_{PD}	OUTPD pull down resistance			1.0		Ω
I_{SOURCE}	High level source current	VSEC = 10 V, R_{ext_pu} = 0 Ω, C_{OUT} = 10 nF, see note 1		2		A
I_{SINK}	Low level sink current	VSEC = 10 V, R_{ext_pd} = 0 Ω, C_{OUT} = 10 nF, see note 1		4		A
Primary Under Voltage Lock Out						
V_{DRV_UV}	V_{DRV} UV threshold, rising	Note 2 Note 3	3.9 9.5	4.15 10.0	4.4 10.5	V
V_{DRV_UVH}	V_{DRV} UV hysteresis	For lower threshold For higher threshold		0.3 0.7		V
Secondary Under Voltage Lock Out						
V_{SEC_UV}	VSEC UV threshold, rising		3.9	4.3	4.8	V
V_{SEC_UVH}	VSEC UV hysteresis			0.3		V

1 *See test circuit in Test Circuit section of datasheet.*

2 *When V_{DRV} is below the UVLO threshold the driver output is actively held low.*

3 *The UVLO trip point is selectable using the SEL pin. See Table 9.*

Table 7: HEY1011 Electrical Characteristics

8.7. Switching Characteristics

-40°C < T_J < 125°C, 7.5 V < V_{DRV} < 15 V, C_{sec} = 22 nF, C_{out} = 1 nF. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Propagation Times						
T_{PHL}	Propagation delay, high to low			50		ns
T_{PLH}	Propagation delay, low to high			50		ns
T_{PM}	Propagation matching	Part to part		5		ns
Rise and Fall times						
t_r	Rise time	R_{ext_pu} = 0 Ω, 20-80%		9		ns
t_f	Fall time	R_{ext_pd} = 0 Ω, 20-80%		7		ns
t_{pw}	Minimum input pulse width that makes output change			50		ns
Startup time						
T_{START}	Wait time before first IN edge is delivered after V_{DRV} is within specification				500	µs

Table 8: HEY1011 Switching Characteristics

9. Applications Information

9.1. Primary UVLO voltage selection

R_{UVLO}	Typical UVLO (V)
Short-circuit	4.15
2.7 kΩ	10

Table 9: HEY1011 UVLO selection

The SEL pin selects the under-voltage lock-out level for the VDRV supply. This is done with an external pull-down resistor from SEL to GND to select the desired nominal UVLO level per Table 9. Detailed UVLO specs are given in Table 7.

9.2. Bidirectional Enable/Disable

EN is a bidirectional open-drain pin which requires a 100k ohm external resistor pull-up to the VDRV pin. The EN pin allows for management of start-up and fault conditions between the PWM controller and multiple HEY1011 drivers, through use of a shared enable EN line. Either the PWM controller or the driver can pull the EN pin low via the EN bus, as shown in Figure 9. When the EN pin is pulled low (either externally or internally), this forces the driver into a mode where the IN pin signal is ignored, and the OUT pins are disabled and actively pulled low. When the EN pin goes high, normal driver operation is enabled.

In the event of an internal driver fault condition, such as UVLO or normal startup delay, the EN pin is actively pulled low internally by the driver. This driver pull-down can be detected by the PWM controller and used as a flag for an external fault, or to flag that the driver is ready, and PWM can commence.

The shared EN line is typically wired-AND with the controller Enable pin, as shown in Figure 9. Multiple HEY1011 drivers can be connected in parallel with the controller on the shared EN line, such that which means that all connected drivers will hold the EN line low until *all* drivers *and* the PWM controller have released their own EN pin, ensuring smooth safe start-up of the system.

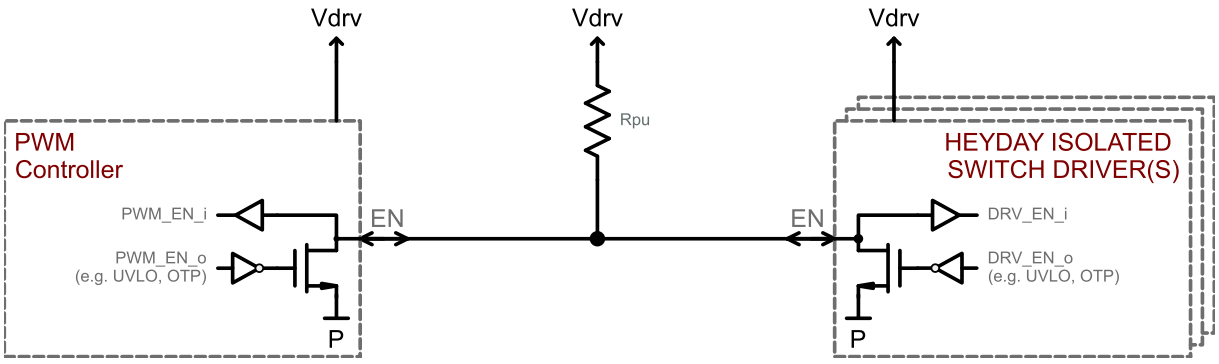


Figure 9: Example 'Wired-AND' connection between driver and controller

9.3. Start-up procedure

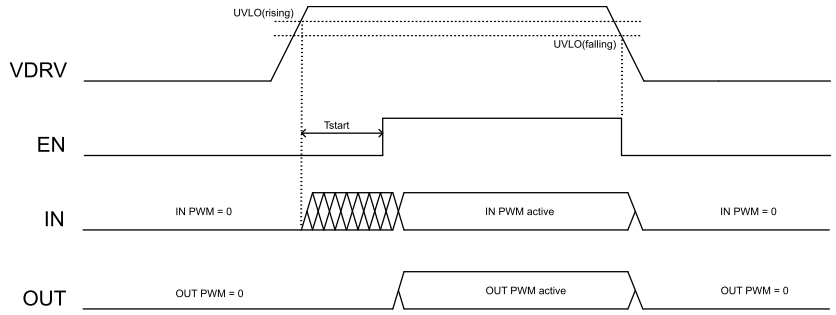


Figure 10: HEY1011 Start-up relationship to be observed between VDRV, EN and IN PWM signal

Any PWM signal applied to IN must remain low until V_{DRV} > UV threshold, to avoid parasitic charging of the V_{DRV} rail through the IN pin internal ESD structures. After V_{DRV} exceeds the UV enable threshold, a startup time delay T_{start} is required, to charge VSEC and allow all internal circuits to initialise and stabilise. During T_{start}, any IN signal inputs are ignored. EN internal pull-down will remain active during T_{start}, and will disable (i.e. go open-drain) only when VDRV has reached its UVLO voltage level, all on-chip voltages are stabilised *and* the internal T_{start} timer has elapsed. This the EN pin can be used via a shared EN line to flag when T_{start} has elapsed, and the driver is ready to respond to PWM signals at the IN pin, as outlined above.

9.4. Operating Frequency

The maximum allowable operating frequency of the HEY1011 is dependent on the operating ambient air temperature, V_{DRV} voltage level, and the gate charge of the external GaN FET being driven at the OUTPU/OUTPD pins. The total power transferred from V_{DRV} voltage on the primary to the external GaN FET on the secondary increases with gate drive switching frequency and V_{DRV} voltage, hence the IC package must dissipate more heat. The safe operating frequency range is shown in Figure 11, along with the stated values for C_{LOAD} (effective capacitive loading due to the external GaN FET gate), C_{SEC} and V_{DRV} voltage.

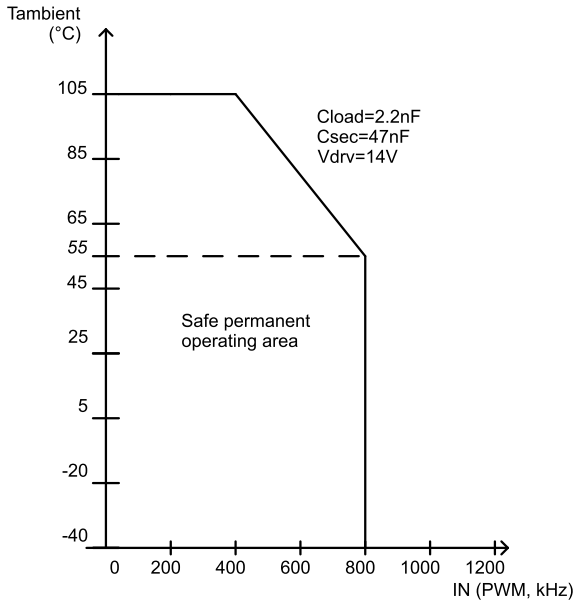


Figure 11:HEY1011 Safe operating PWM frequency versus ambient air temperature

9.5. V_{DRV} and C_{SEC} Design Guidelines

The output gate drive amplitude is always less than the V_{DRV} voltage.

The OUTPU gate voltage level depends on factors such as V_{DRV} level, C_{LOAD} and C_{SEC}. Figure 12 shows the typical output gate drive amplitude as a function of V_{DRV} and C_{LOAD}, for an assumed value of C_{SEC} as a multiple of C_{LOAD}, for a 50% duty cycle PWM at the IN pin.

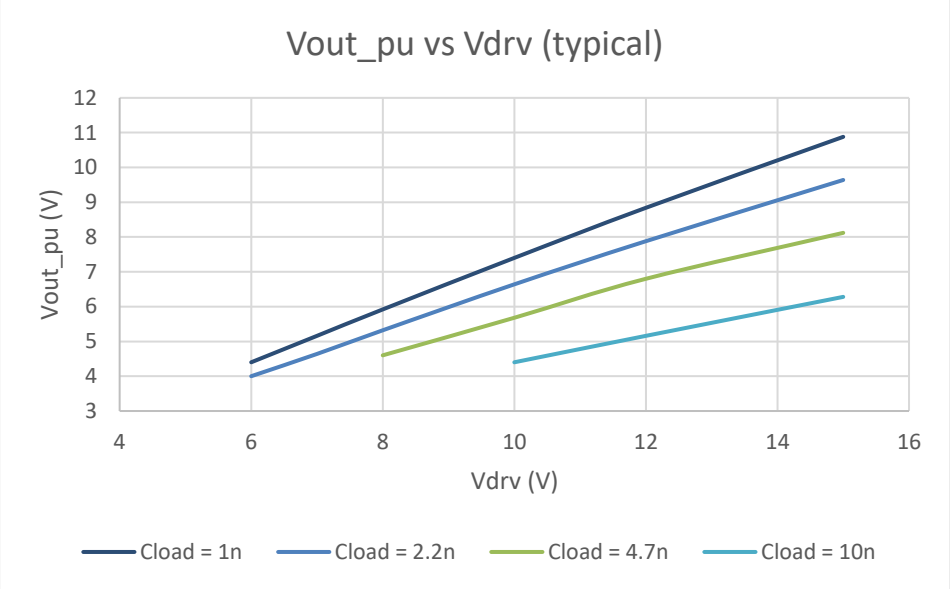


Figure 12: Typical Vgate voltage versus Vdrv voltage for 4 Cload capacitors

*Conditions: F_{IN} =100kHz, D = 50%, UVLO = 4.15V, C_{SEC} = 20*C_{LOAD}*

Figure 13 shows the minimum expected output gate drive amplitude as a function of V_{DRV} and C_{LOAD}, but for minimum IN pin PWM pulse-width on-time (and under similar assumptions of C_{SEC} as a multiple of C_{LOAD}).

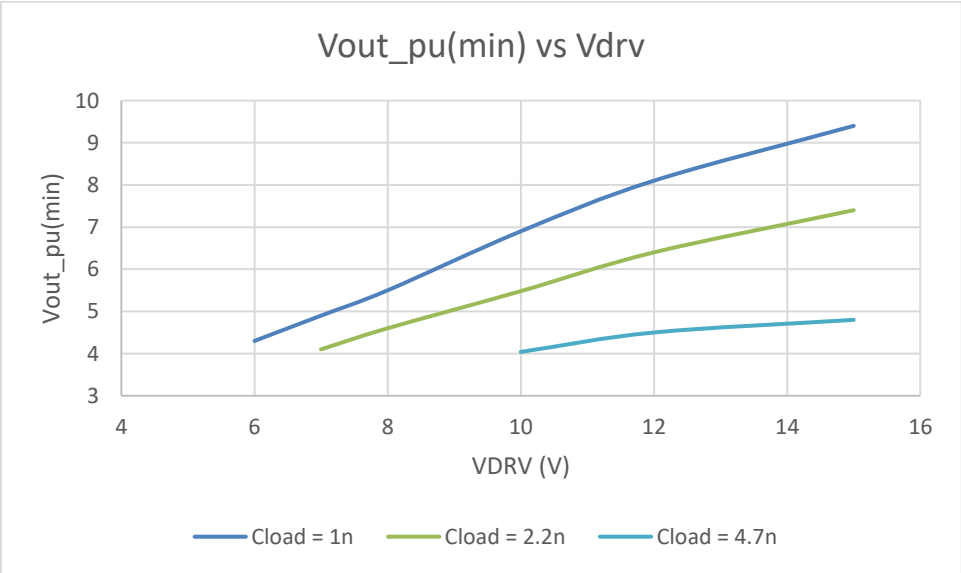


Figure 13: Minimum Vgate voltage versus Vdrv voltage for 4 Cload capacitors

*Conditions: F_{IN} =120kHz, T_{IN-ON} = 50ns, UVLO = 4.15V, C_{SEC} = 20*C_{LOAD}*

The following operating values for C_{SEC} are recommended to ensure optimal operation:

C_{Load}	C_{SEC}	Minimum V_{DRV}
1 nF	22 nF	7.5 V
2.2 nF	22 nF	8.5 V
	47 nF	8.5 V
4.7 nF	47 nF	10.5 V
	100 nF	10.5 V
10 nF	100 nF	15 V

Table 10: suggested C_{SEC} and V_{DRV} values

These suggestions consider the typical and worst-case use cases. The suggested C_{SEC} and V_{DRV} provide a minimum of 5 V on the OUTPU pin regardless of the input pattern.

The C_{SEC} value associated with each C_{LOAD} is given as a recommendation. Many values are possible, but it is recommended that C_{SEC} is at least ten time larger than C_{LOAD}. Larger C_{SEC} will require a longer starting time. The maximum recommended value of C_{SEC} = 100 nF should not be exceeded.

9.6. Bipolar Output Drive

Bipolar output drive is used to provide a negative gate voltage which can be beneficial in protecting against false turn on due to parasitic circuits components. It can be added simply to the HEY1011 by including three extra small external components. For full details see the Heyday application note HD-000222-AN.

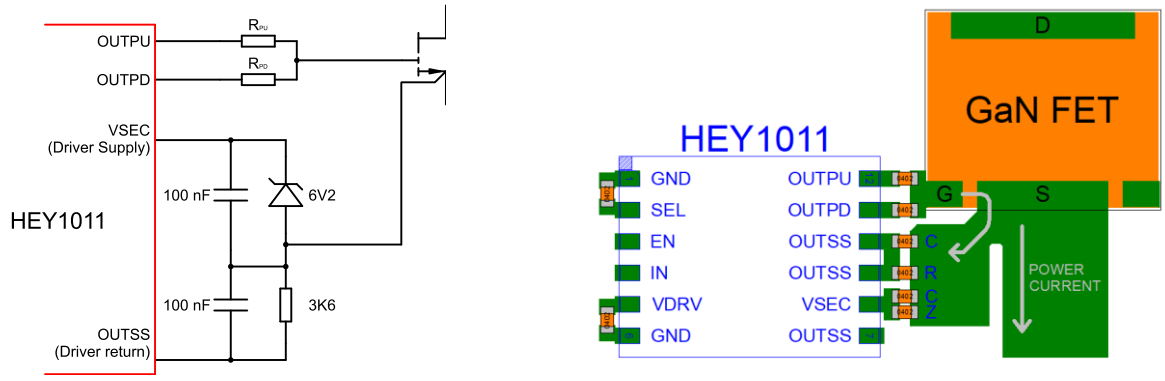
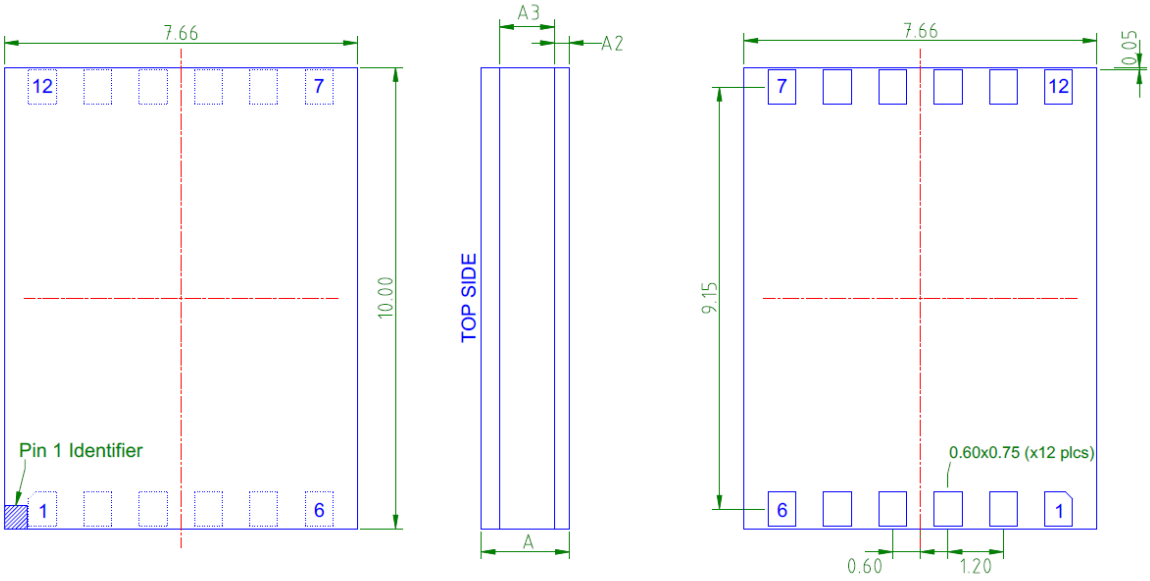


Figure 14: HEY1011 Bipolar drive and recommended PCB layout

10. Package Outline



Dimensional Ref.			
Ref	Min	Nom	Max
A	1.81	1.91	2.01
A2	0.28	0.32	0.36
A3	1.2 Basic		

Figure 15: HEY1011 Package Outline

11. Recommended PCB Footprint

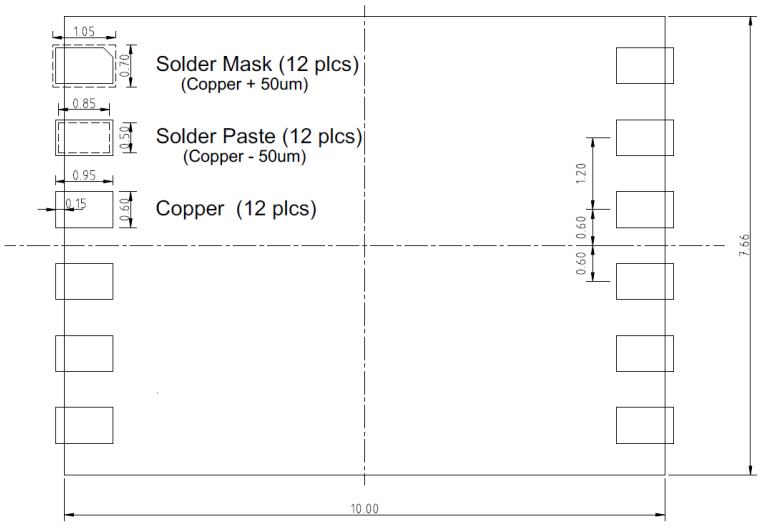


Figure 16: Recommended PCB footprint

12. Regulatory information (pending)

12.1. Safety Certification Standards

- UL1577 Component safety (optical and digital isolators)
- VDE0884-11 Component safety (digital isolators)

Specification Parameter	Target Specification	Specification detail and comments
V_{ISO}	5700 V_{RMS}	Withstand isolation voltage per UL 1577
V_{IOTM}	8000 V_{PK}	Maximum transient isolation voltage per VDEE0884-11
V_{IORM}	630 V_{PK}	Maximum working isolation voltage
C_{IO}	< 1 pF	Barrier capacitance, two terminal device connection
R_{IO}	> 10^{12} Ω	Isolation resistance, two terminal device
DTI	> 450 μm	Distance through insulation
Creepage	> 8 mm	External package creepage
Clearance	> 8 mm	External package clearance

Table 11: Target Regulatory Specifications

13. Ordering Information

Driver	Switch	#channels	Output	Isolation	Package
HEY1011-L12N	GaN driver	1	Unipolar	Functional	LGA 12 pin
HEY1011-L12A	GaN driver	1	Unipolar	Isolated	LGA 12 pin

Table 12: Device ordering information

14. MSL rating

Device	MSL Rating	Maximum floor life at standard ambient (30°C/60%RH)	Maximum peak reflow temperature	Pre-reflow bake requirement
HEY-1011-L12C Alpha samples	MSL-3	168 hours	165°C	Per JEDEC J-STD-033C
HEY-1011-L12 Production devices	MSL-3	168 hours	260°C	Per JEDEC J-STD-033C

Table 13: MSL and maximum peak reflow temperature

Per JEDEC J-STD-033C, the HEY1011-L12 devices are rated MSL3. This applies to both advance Alpha samples (HEY1011-L12C) and final production release devices.

This MSL3 rating means that once the sealed production packaging is opened, the devices must be reflowed within a "floor-life" of 168 hours (1 week) if they are stored in under standard ambient conditions (30°C and 60% relative humidity (RH)).

The peak reflow temperature should not exceed the maximum specified in Table 13.

If the devices are exposed to the standard ambient for more than 168 hours, they must be baked before reflow, to remove any excess moisture in the package and prevent damage during reflow soldering. The required bake times and temperatures are detailed in IPC/JEDEC standard J-STD-033C.

If the devices are exposed to higher temperature and/or RH compared to the standard ambient of 30°C/60% RH, the floor-life will be shortened due to the increased rate of moisture absorption. If the actual ambient conditions exceed the standard ambient, it is recommended that parts should always be baked per IEC/JEDEC J-STD-033C before reflow, as a precaution to avoid potential device damage.

15. Disclaimer

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