Simple technique measures performance of GaN-based power supplies

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Today, most power supply roadmaps have GaN transistors incorporated into them as a key platform. The advantages of GaN transistors compared to Si MOSFETs, IGBTs, and SiC MOSFETs means engineers are extensively designing them into their systems. However, these advancements with GaN transistors in switching power supplies have also made characterizing the performance of these power supplies increasingly challenging. Measuring the high-side V_{GS} in a half bridge, which is a traditional way to diagnose transistor cross conduction, can be a demanding task for a GaN-based design. The typical solution is to use high-cost measurement equipment, which does not always produce useful results. This article demonstrates an easy and cost-effective method using the unique characteristics of GaN transistors to measure cross conduction.

Half-bridge and full-bridge configurations used for synchronous rectification in boost or buck converters and bidirectional converters use complementary drive signals for the high- and low-side transistors. The drive signals must include a small amount of "dead time" between the period when one transistor in the half-bridge turns off and the other transistor turns on, to ensure the transistors do not cross-conduct. Cross conduction occurs when the transistors in a half-bridge configuration are on simultaneously, a condition that increases losses and is potentially damaging to the transistors. Increasing the dead time helps protect the transistors but it also creates another type of loss that occurs when both transistors are off that reduces the bridge's efficiency and lowers the available duty cycle range of the power converter. As a result, minimizing the bridge's dead time while ensuring no cross conduction occurs is a key design goal. Verifying this operation is the challenge.

The common method to verify proper cross-conduction operation of a power supply half-bridge topology is to verify the dead time between the high-side and the low-side driving signals simultaneously using two probes. Measuring GaN transistor drive signals, especially the high-side gate, is challenging, and often causes mis-triggering, frustrating design engineers.

The gate signals for GaN devices have high slew rates, in the order of 1V/ns, which poses a challenge for high-side measurement using conventional isolated probes. If the measurement system does not have sufficient common mode rejection ratio (CMRR), the rapidly changing common mode voltage of high-side source node results in interference, which obscures the measurement. Also, the parasitic capacitance introduced by traditional passive voltage probes can distort the gate drive signal, causing cross conduction.

Optically isolated measurement systems, such as the Tektronix TIVH Series IsoVu, have been developed with DC CMRR greater than 160 dB to provide achievable high-side V_{GS} measurement solutions. Such measurement systems must also minimize the sensing loop area and provide an enhanced shielded measurement signal path. Doing so requires that the power converter circuit board design includes probe points equipped with specialized connectors, like micro-miniature coaxial (MMCX) connectors, that provide low-capacitance access to critical signals. **Figure 1** shows the result of high-side V_{GS} measurement and the double pulse test board using GS66516T GAN transistors. The TIVH Series IsoVu and MMCX connectors were used to achieve this, as shown in **Figure 2**.

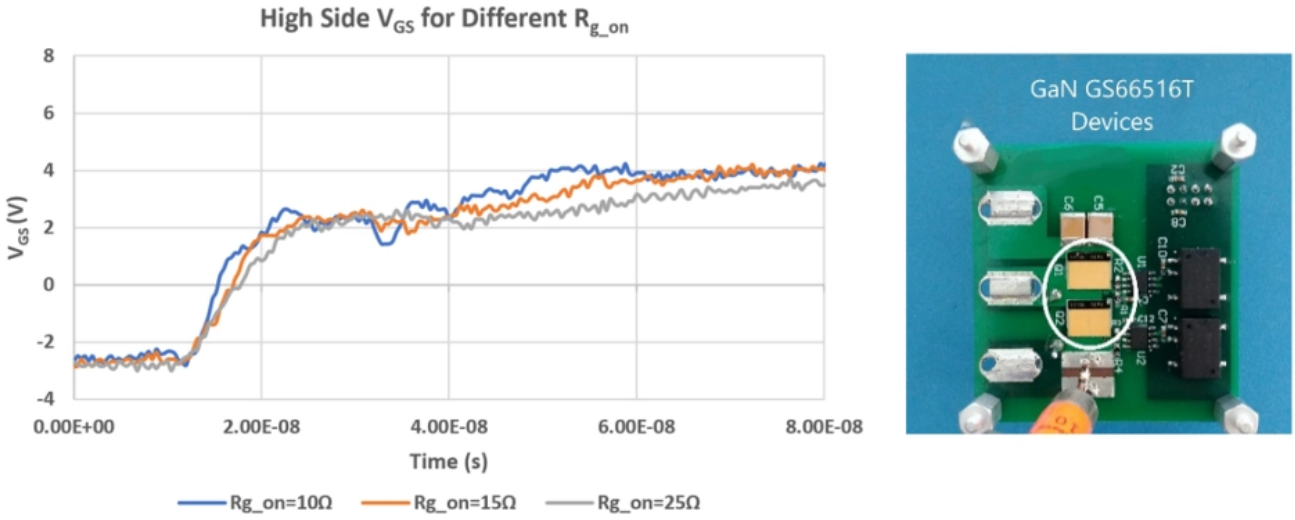

Figure 1 The graph on the left shows the measured high-side V_{GS} at I_{Load}=23A for different R_{g_on}, using the Tektronix IsoVu measurement system. The GS66516T double pulse test (DPT) board is shown on the right.

Figure 2 The measurement setup includes the IsoVu system (left) and a DPT board with MMCX connectors (right).

The cost of the measurement system and the additional complexity and sensitivity of the signal path has left room for more cost-effective and less-sensitive solutions. A method developed by engineers at GaN Systems measures only the low-side transistors, addressing these concerns.

A typical hard-switching turn-on transition schematic diagram of a GaN half-bridge is shown in **Figure 3**, with the representative low-side I_D curve shown in **Figure 4**. During the voltage commutation period (Figure 3d), the voltage across S_1 increases and the voltage across S_2 decreases. Accordingly, the transistor drain-to-source capacitors C_1 and C_2 will be charged and discharged, respectively. Since the two-dimensional electron gas (2DEG) channel of S_2 is conducting and the 2DEG channel of S_1 is turned off, C_1's charging current flows through S_2 and will result in a current bump.

Figure 3 These hard-switching transition diagrams show S_1 conducting (a), dead time (b), current commutation (c), voltage commutation (d), and S_2 conducting (e).

Since GaN transistors, unlike Si and SiC MOSFETs, do not have inherent body diodes and therefore there is no reverse recovery loss during the voltage commutation (t1~t2 in Figure 4). The bump area of the low-side drain current is a result of the capacitance (C_{OSS}= C_{GD} + C_{DS}) charging current, $I_{Q(OSS)}$, from the opposite switch S_1.

Figure 4 This is the hard-switching turn-on procedure of a low-side GaN transistor.

If cross conduction does occur, the current bump area will be greater than what is expected from the C_{OSS}. Cross conduction can happen during, after, or during and after voltage commutation simultaneously (**Figure 5**).

Figure 5 Cross conduction occurs during, after, or both during and after voltage commutation.

Next page: Determine if cross conduction exists