



GaN IN CLASS-D AUDIO

Advantages with GaN Systems –
A Comparative Look

GaN Systems White Paper
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Introduction

The high performance of GaN Systems transistors in Class-D audio amplifiers is demonstrated in the GaN Systems Class-D Audio technical manual.

It is difficult to compare the GaN Systems' results to the published efforts of Silicon MOSFET or other GaN-based solutions for a number of reasons. Among them are:

- 1) Measurement Test Benches are not defined
- 2) Measurement Conditions are optimized for a given measurement (and not specified)
- 3) Test Platforms represent highly optimized versions of the Competitive amplifier design
- 4) Test Measurements focus on the "best possible picture" parameters
- 5) Special Test Measurements often reflect individual preferences

For example, THD may or may not include the Noise component (THD+N), although THD+N is the established criterion. THD+N measurements vary with Power Output, Frequency, Load, Power Supply Voltage, and Temperature. This variation can extend over a 10:1 range, depending on the criteria and the Test Bench measurements.

However, it is possible to compare the various GaN and Silicon transistor approaches to Class-D Amplifier topologies if we assume that the devices are applied in somewhat equivalent methods. In some cases, it is these methods that become the major areas of differentiation.

Class-D Amplifier Transistor Approaches

The comparisons will be considered in each of the following areas of differentiation:

- 1) Device Parameters and Characteristics
- 2) Performance (Both Audio and Thermal)
- 3) Application Circuit Complexity including Device Driver Considerations
- 4) Ease of Manufacturing (Process Risks)

For these comparisons, the following options were considered:

- 1) GaN Systems Devices
- 2) GaN Competitor #1 Devices
- 3) GaN Competitor #2 Devices
- 4) Silicon FET Competitor Devices

Device parameters and characteristics

Specification	GaN Systems	GaN Supplier B	GaN Supplier C	Silicon Supplier
Operating				
V _{DS} Max	100V	100V	400V ⁽⁵⁾	100V
I _D Max	90A	18A	31A	25A
I _D Pulse Max	140A	75A	60A	45A
Parameter				
R _{DS(ON)}	8	12	70	16
Q _{Gate}	8	3.4	4.5	10
Q _{rr}	0	0	0	19
Q _{OSS}		16	35	20
Size		3.4mm ²		10.9mm ²
Package	GaNPX[®] <i>embedded</i> ⁽¹⁾	LGA ⁽²⁾	HSOF-8 ⁽³⁾	DirectFET ⁽⁴⁾

(1) Near chip-scale embedded power package

(2) Solder Ball on Die Flip-Chip

(3) Large QFN-Style

(4) Custom Metal-Can Style

(5) Lowest Available Voltage for Class-D Application (see impacts later in this document)

Parameter/Spec	GaN Systems GaN Class-D Design	GaN Supplier B GaN Class-D Design	GaN Supplier C GaN Class-D Design	Silicon Class-D Design	Typical Consumer Product**	Typical Professional Product**
Voltage Rating	100V	100V	400V ⁽⁵⁾	100V	N/A	N/A
THD+N (1kHz)					< 0.05%	< 0.1%
@ 1/10 Power	0.004%*	0.01%*	0.05%*	0.015%		
@ 1/8 Power	0.005%*	0.008%*	0.02%*	0.005%		
@ 1/3 Power	0.018%	0.006%	0.006%	0.007%		
@ Full Power	0.018%	0.03%	0.008%	0.02%		
THD+N (-9dBFS)					< 0.1%	< 0.2%
@ 100Hz	0.002%*	0.004%*	N/A	0.003%		
@ 1kHz	0.005%	0.006%	0.006%	0.007%		
@ 6.7kHz	0.03%	0.03%	N/A	0.040%		
SNR/DNR					> 108dB	> 110dB
Open-Loop	116dB	116dB	N/A	N/A		
Closed-Loop	105dB	103dB	104dB	101dB		
Efficiency***					> 80%	> 85%
@ 8 ohms	94%	96%	90%	90%		
@ 4 ohms	92%	92%	90%	85%		
Freq. Response	20Hz ~ 20kHz	20Hz – 20kHz	20Hz – 20kHz	20Hz – 20kHz	20Hz – 20kHz	20Hz – 20kHz

*Note: Performance Measurements dominated by the Noise Floor

**Note: Representative of the “Mid to High-End” of the market

***Note: Includes loss of Efficiency due to other Amplifier components

Performance

Often, these types of values never tell the whole story. It is the understanding of how all of these performance parameters interact and are dependent on each other that allows for the more complete appreciation for the technologies. Examples:

- 1) The Output Filter of the Class-D Amplifier is designed to allow for the highest in audio fidelity. The 20kHz upper-end Frequency Response is limited by the Front-end Pre-Amp and Sample Rate Converters. This is not a limitation for the GaN Amplifier itself. For the GaN Systems Class-D Design, $L = 10\mu\text{H}$, $C = 0.82\mu\text{F}$, results in the -3dB point at 56kHz.
 - a. The load impedance will affect the Q of this Output Filter and hence the shape of the Filter prior to the 56kHz roll-off point. With 8-Ohms, the Q is about 1.14. This will create a slight 'peaking' in the Frequency Response at around 20kHz. With 4-Ohms, the Q is half that at about 0.57. This will introduce a slight 'sag' in the Frequency Response at the 20kHz point.
 - b. The GaN Systems design targets a Butterworth Response, assuming a 5-ohm Output Load Impedance (best compromise between the various and typical speaker load impedances and considering component tolerances). This allows full bandwidth Frequency Response to 40kHz, demonstrating superior performance.
- 2) The THD+N vs. Level measurements are heavily influenced by the Noise Floor, which almost always introduces an increased THD level as the audio signal is reduced.
- 3) THD+N vs. Level and THD+N vs. Frequency are both dependent on the deadband timing. However, the deadband timing also affects the Efficiency – especially at lower power levels.
- 4) For THD+N vs. Frequency, there is a reason for the choice of 6.7kHz as one of the measurement points for this Table. When using an Audio Precision Analyzer, it is desirable to utilize the internal AES17 Filter, or an equivalent Filter that eliminates or reduces any Noise or Distortion components that are outside the audio frequency band that could potential be aliased back into the audio spectrum. The 6.7kHz would represent the initial frequency at which the 3rd Harmonic distortion component could be eliminated or reduced by this AES17 Filter. Even in closed-loop (feedback-based) designs, this would be obvious, as seen in Figure 1 below.

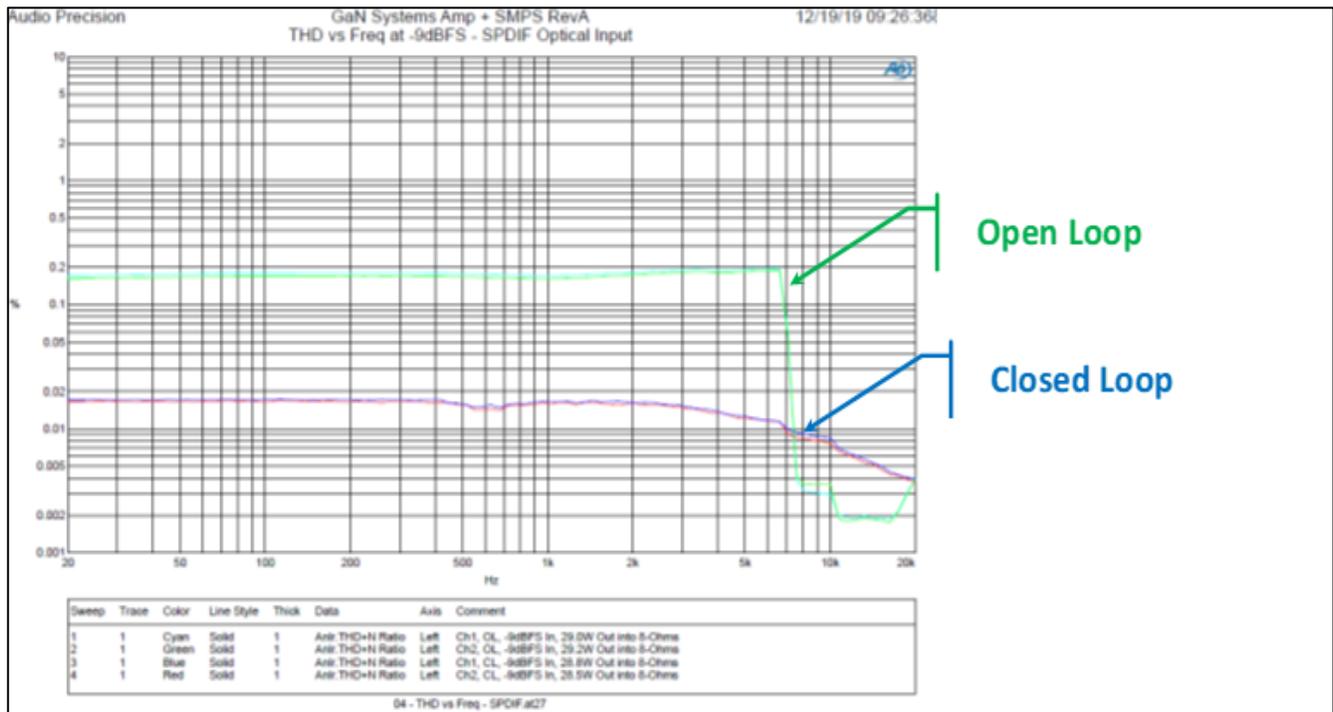


Figure 1: THD+N vs. Frequency (@ -9dBFS) Performance Plots

As captured, it is immediately obvious in the Open-Loop Plot where this 3rd Harmonic Distortion component is eliminated.

The important observations from these plots, which are extremely important characteristics of the GaN Systems Class-D Amplifier design, are:

- The THD+N vs. Frequency Plot is virtually flat indicating no increased distortion as the Frequency is increased.
- This is further evident in observing the range between 6.7kHz and 10kHz (where the 2nd Harmonic Distortion component is affected) and beyond 10kHz, where the Distortion Plot is still virtually “flat” with only these specific Distortion components removed.
- It is also important to note that the Closed-Loop Plot remains relatively “flat” even beyond 6.7kHz. Again, this is characteristic of the GaN Systems Amplifier implementation because when all trade-offs are considered the results are best of the competitive comparison solutions.

This performance with the GaN Systems GaN FET technology is achievable without compromising or otherwise sacrificing when these important trade-offs are made.

While the Efficiency appears to be slightly lower than that of GaN Supplier B, a more careful examination of the Efficiency Plots indicates that even with these optimization trade-offs, the Efficiency at lower Output Power levels is relatively higher, which indicates that these trade-offs have resulted in a new optimization of switching loss versus conduction loss. This is reflected in lower losses under ambient or idle conditions, further reducing the need for any heat sink or heat elimination component.

To provide guidance of how these device parameters and characteristics affect the Audio Amplifier performance parameters, see the associated performance capture below.

When considering the advantages and disadvantages of the various approaches, there is typically a trade-off between price and performance. These parametric and parasitic components are highly dependent on the fabrication process for the individual devices. For this reason, it is always best to choose a device whose operational parameters closely match those required by the application (Voltage, Current, $R_{ds(on)}$, etc.).

For instance, the use of a 400V FET in an application that requires only a 100V FET results in increased complexity of the FET driver design, as well as opportunity for increased switching loss that is introduced by the increased parametric and parasitic elements of the device itself. The increased complexity can readily be seen in the Gate Drive Schematic captured in Figure 11 below. This increased complexity is required to offset the increased parametric and parasitic contributions also listed for GaN Supplier C above in the Device Parameter Table.

The 400V devices are applicable in audio markets that require much higher voltage outputs that are characteristic of the Constant Voltage Amplifier designs for Professional, Commercial, and Industrial sound system applications. These applications require Output Voltage swings of 70V_{rms} to 100V_{rms} with arrays of loudspeakers connected to single Amplifier outputs. However, even these Output Voltage swings could easily be accommodated with much lower voltage devices where the compromise in performance is much less of an impact.

Perhaps the most touted advantage of GaN technology over standard Silicon MOSFET technology is the improvement in efficiency of the switching Power Stage. The extremely high efficiency of the GaN Systems Power Stage is demonstrated in Figures 2 and 3. For the first plot (blue) captured in Figure 2 and Figure 3, this “Idle Dissipation” was subtracted from the overall dissipation. This is the appropriate approach as this “Idle Dissipation” does not factor into the “Efficiency” of the GaN FET Power Stage. It also does not prove to be a significant contributor to the overall Efficiency at the power levels which would create the need for costly components such as heat sinks and large copper mounting tabs. For comparison purposes, the second plot (red) of each Figure adds back the additional power loss that is characteristic of the total Class-D Amplifier Test Platform, but does not include the peripheral dissipation associated with components that are not a part of the Amplifier Platform.

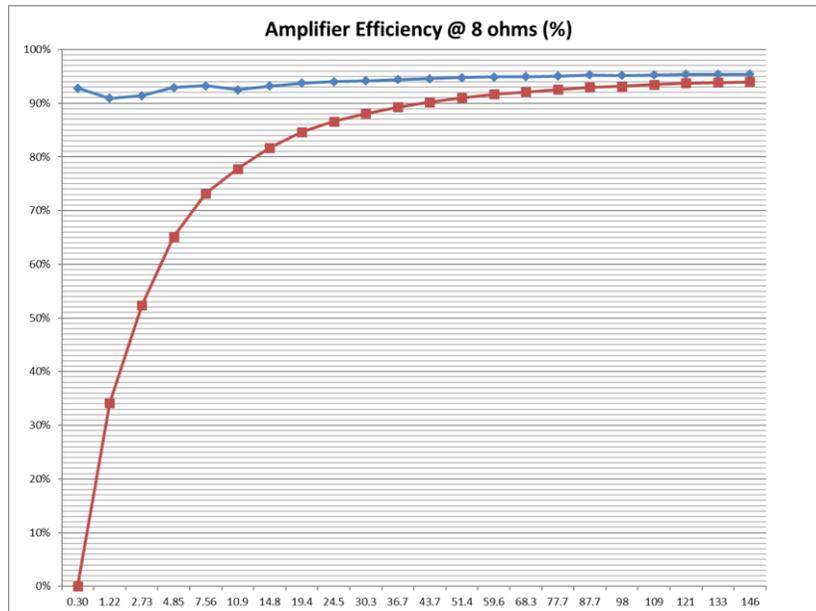


Figure 2: Closed-Loop Amplifier Efficiency vs. Output Power @ 8 Ohms

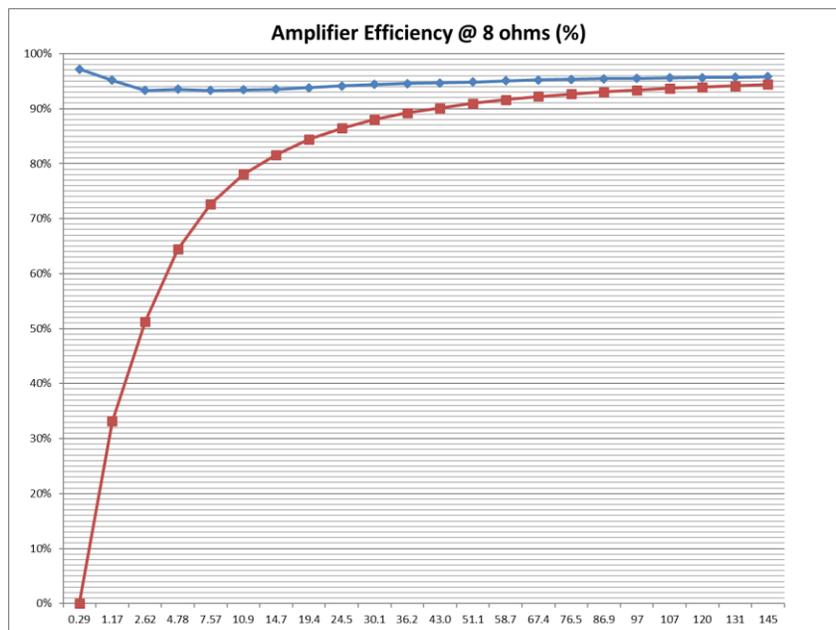


Figure 3: Open-Loop Amplifier Efficiency vs. Output Power @ 8 Ohms

The blue curve in each plot indicates the Efficiency of the Power Stage and should be used when comparing the GaN FET Efficiency with other MOSFET or Integrated Power Device solutions. The red curve in each plot indicates the Efficiency of the GaN-based Class-D Amplifier and should be used in comparison with other MOSFET Reference Designs (that are measured equivalently) or Integrated Power Amplifiers (of equivalent Power Output capability).

Comparable efficiency plots for GaN Supplier B are shown below in Figure 4.

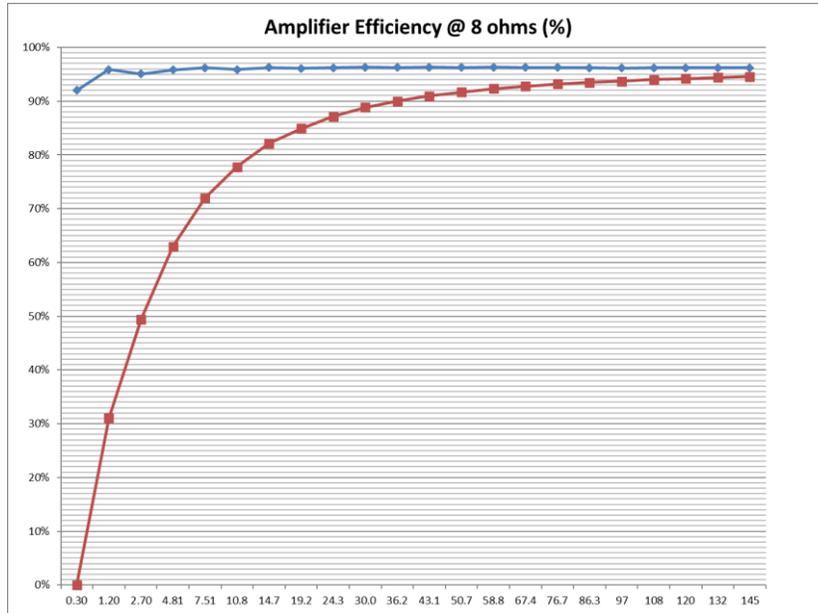


Figure 4: Comparable Efficiency Plot for GaN Supplier B

Similar to the GaN Systems solution, any properly sized and selected GaN FET Power Stage competitive solution should provide excellent thermal performance and significant improvement over the Silicon FET counterpart. However, if the devices are not properly sized and selected for the application, the efficiency as well as other performance factors can be significantly impacted as shown in a comparable efficiency plot below for GaN Supplier C.

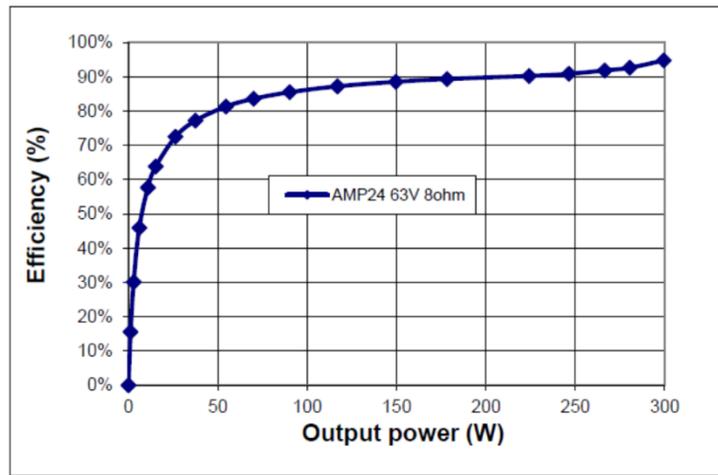


Figure 5: GaN Supplier C Efficiency Plot

While this efficiency plot is still very good, it sacrifices at least 5%-6% of potential efficiency improvement from the more appropriately sized devices. This is because the optimal thermal performance of any switching device is a trade-off between switching loss and conduction loss.

As a result, the efficiency plot for these devices is very similar to that of a standard Silicon FET implementation, so this particular advantage of using the GaN FET technology is seriously compromised.

The primary goal in the performance of any Class-D Amplifier – as with any Audio Amplifier – is the transparency of audio replication, or the attempt to replicate most closely the recorded or performed audio. With a ‘switched amplifier’ system, such as with Class-D, one of the main amplification goals is to use a ‘perfect’ switching waveform. The further from ‘perfect’ the switching waveform is the further from ‘perfect’ the audio replication will be. It should also be noted that in a Class-D PWM (Pulse-Width-Modulated) Audio Amplifier, this switching waveform must remain ‘perfect’ over the entire modulation range (or Modulation Index). In the following discussion, it can be readily seen that the ‘imperfections’ of the switching waveform are much more impactful at the extremes of the modulation where the switching waveform is perhaps only 5% to 10% of the entire switching cycle. The following images illustrate the impact of the imperfections that are usually present in a PWM-style amplification solution.

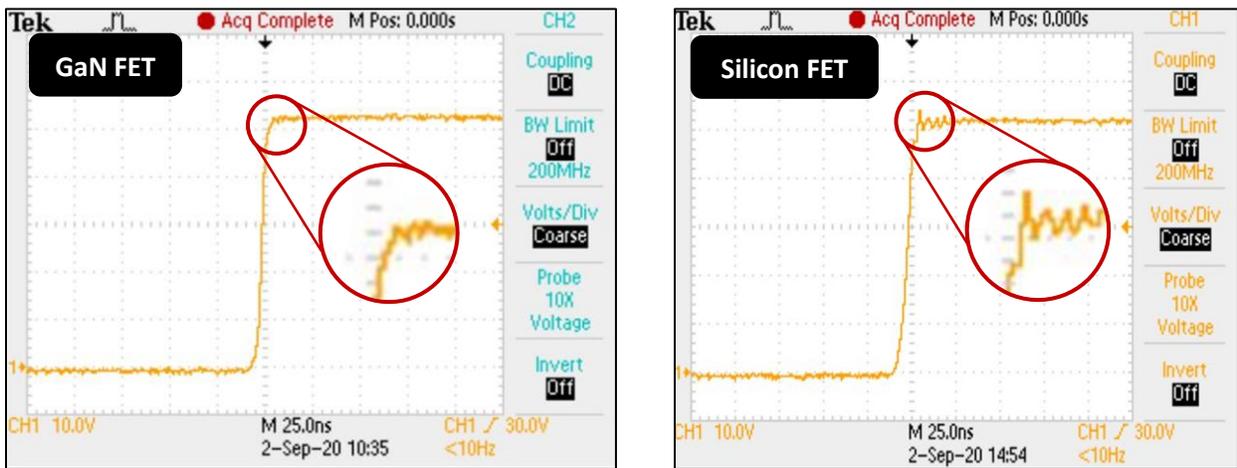


Figure 6: Switching Waveform Comparisons: GaN FET waveform (left) and Silicon FET waveform (right)

Each of the imperfections of this switching waveform can be directly tied to a parameter or characteristic of the power transistor devices used in the modulated amplification power stage. The effects of capacitive or ‘charge-based’ parameters for Silicon FETs are shown in Figure 7a below; the undesirable impacts to the waveform and hence, sound quality, are apparent.

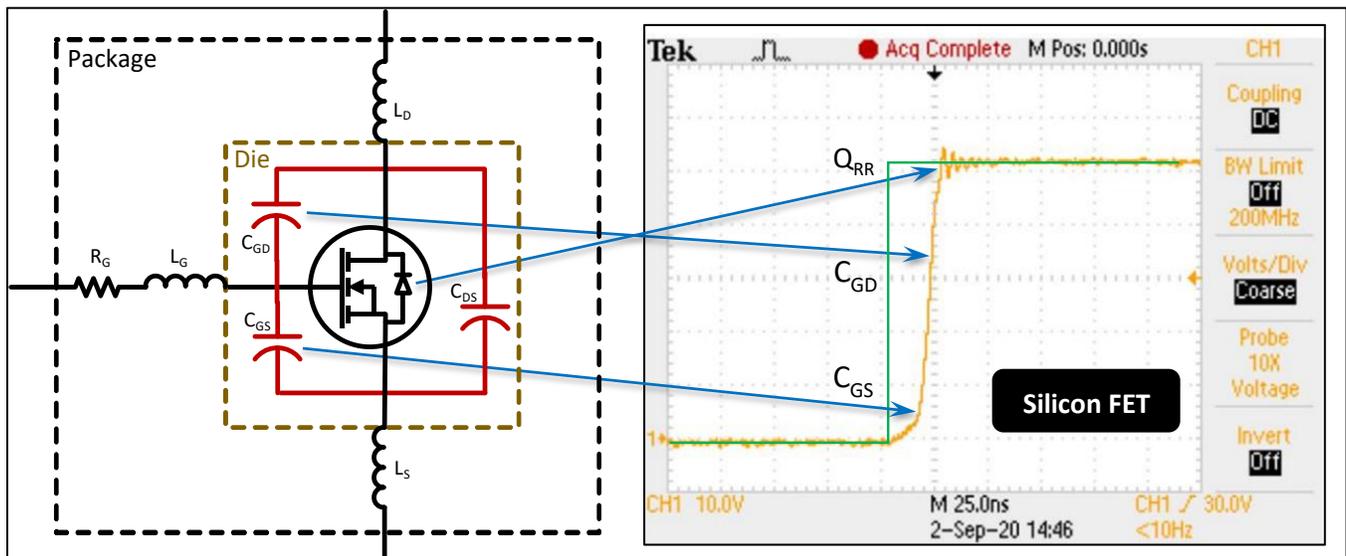


Figure 7a: Charge-Related Parametric Influencers Negatively Impacting Silicon Switching Performance

A similar analysis for GaN FETs shows a much more square shape signal with much smaller charge-related influencers and no Q_{rr} losses resulting in a more superior sound reproduction.

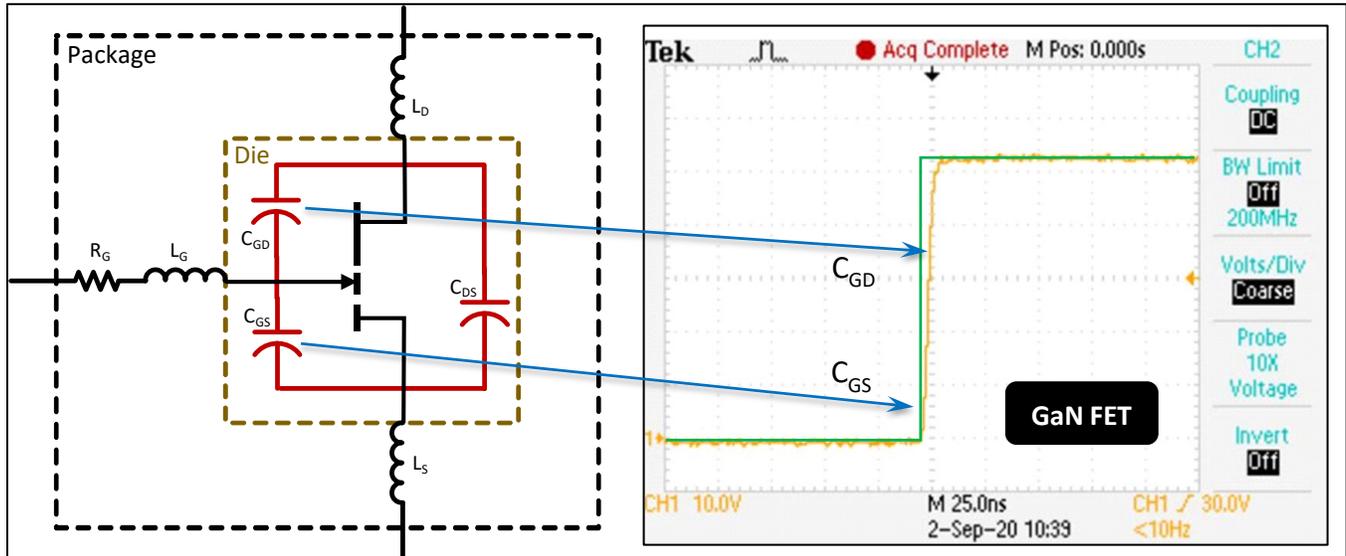


Figure 7b: No Q_{rr} and very small charge related influencers with the GaN FET

The system-level, non-charge-related parametric variations and differences also influence the achievable performance. The figure below shows the Silicon FET and GaN FET transistor performances, as compared to the “Ideal” switching waveform (green line). The green square wave line ‘turn-on’ and ‘turn-off’ are representative of the actual PWM Control signal that is sent to the transistor. Compared to the GaN FET, the Silicon FET has significant ‘turn-on’ and ‘turn-off’ delays resulting in degraded performance.

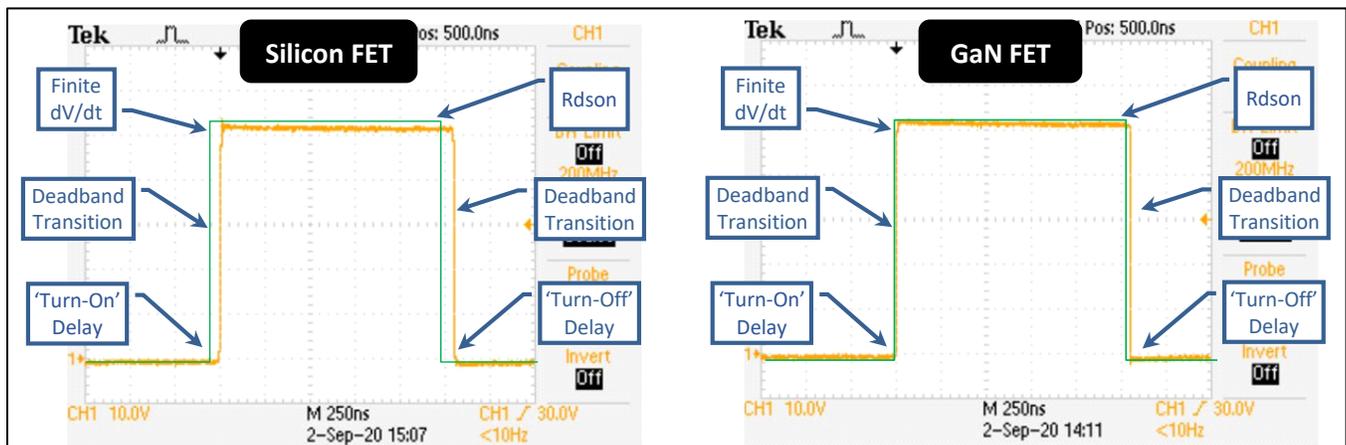


Figure 8: Non-Charge-Related Parametric Influencers: Silicon FET waveform (left) GaN FET waveform (right)

Ease of Manufacturing

These combined parametric imperfections are then exacerbated by the required PCB layout constraints that are forced in attempting to minimize the associated performance anomalies. These PCB layout constraints are further complicated by the necessity to include and

implement the various fault and application protection methods for the ‘real-world’ uses of these technologies. With the necessity to integrate very closely and ‘tightly,’ these fault isolation and recovery mechanisms highlight the importance of packaging and package-driven constraints.

Even with the most ideal parametric situation, the physical implementation of the amplifier switching Power Stage carries the burden of these same constraints in the form of parasitic elements on and within the PCB layout and associated component placements.

The various packaging types for the competitive landscape are shown below.



Figure 9: GaN FET package variations

While some of these packaging alternatives seem to offer a smaller, more real estate-sensitive approach, it comes that the price of both manufacturability and thermal management. Even though the GaN devices offer a much higher efficiency at the power levels needed for these applications, the thermal solution is still important and the thermal mass of the individual devices play into the ability to sense and manage any heat-related issues. Unfortunately, not all application spaces are comfortably managed at 25°C. The manufacturing restrictions can force the PCB implementations into more expensive processes, sometimes outweighing the advantage of reduced heat sink costs.

While the GaN Systems packaging is only slightly less sensitive to PCB real estate, the increase in simplicity of manufacturing and assembly make it a very desirable compromise. In addition, the GaN Systems implementation offers a discrete and separate Kelvin connection to the Gate of the GaN FET which greatly simplifies the PCB Layout required to achieve the very best ‘return path’ for efficient Gate Drive. As can be seen from the earlier spreadsheet comparison, one of the major hardware design differences is in the method for driving the Gate of both the GaN Device and the Silicon FET.

Application Circuit Layout

The Silicon FET Drive is perhaps best understood, but it still requires some additional thought in providing a separate power supply to the FET Driver, and in adjusting the deadband timing for each Half-Bridge Power Stage. A typical Gate Drive circuit for a Silicon FET design is shown below in Figure 10.

simply because the need to accommodate the required layouts for a non-esoteric fabrication process often offsets these improvements.

In particular, the inductance in the Gate Drive is significantly reduced in a 'direct die' attachment package, a critical element in GaN Devices, which can switch much faster than their legacy Silicon counterpart. However, as mentioned, this packaging approach introduces constraints in the PCB Layout and Fabrication/Manufacturing processes that are not as friendly to some mainstream processes.

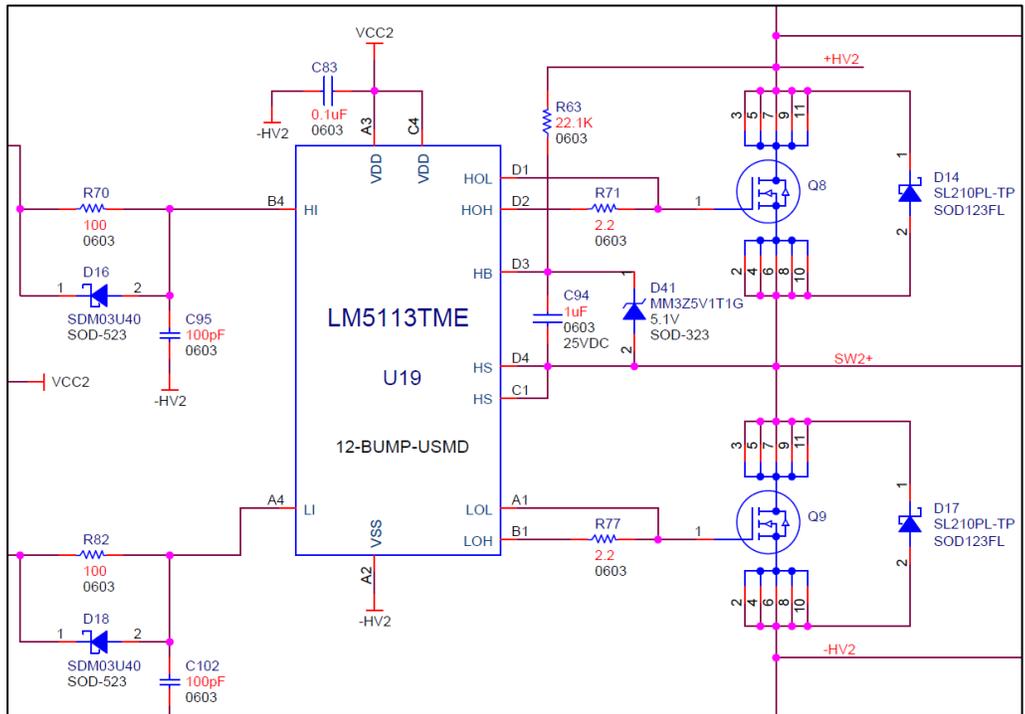


Figure 12: GaN Device Supplier B Gate Drive Circuit

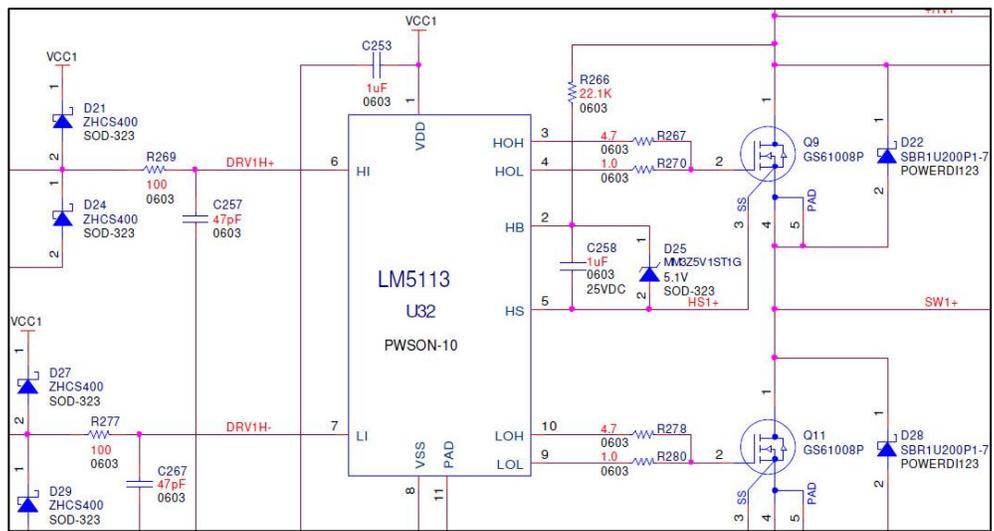


Figure 13: GaN Systems Typical Gate Drive Circuit

Another technique to offset the inductance of the Gate and its effect on the switching characteristics is through the addition of a “Kelvin” connection to the Gate Driver return, as provided by the GaN Systems devices. This “Kelvin” connection not only provides a very low inductance return for the Gate Drive, but also isolates this return from the much higher current of the Source where most devices establish their Gate Drive Return. When working with THD and Noise measurements that are down by 110dB, even very small perturbations of this Gate Drive, either caused by the bond wire or attachment inductance or by the perturbations induced by the Source currents, can influence these measurements significantly. In addition, the increased ‘jitter’ due to the induced uncertainty of the switching will also impact the sonic or audio performance of the Amplifier. This is not so crucial in a Power Supply or Charger application but can be significant in a high-performance Audio Amplifier implementation. With all constraints considered and with the additional inclusion of the “Kelvin” Gate connection, the GaN Systems implementation offers the very best option for optimizing each of these Gate Drive considerations. As seen in Figure 13, the design is compact and simple, and the resulting PCB Layout is easily achieved with Design Rules that can be accomplished by most any high-quality PCB fabrication shop.

Summary

The comparative study points out that GaN FET technology offers a better and more efficient solution for most ‘switching technology’ applications. However, this does not necessarily mean that all GaN FET technologies and devices are equally applicable to Class-D Audio Amplifier applications. As a matter of fact, of all the GaN FET devices that are available (along with the complimentary Gate Drivers that truly work in this harsh environment), only few have been proven to work well in an Audio Amplifier application. The reason for this is simple. A Class-D or PWM Amplifier design forces constraints on the switching Power Stage that are not required in any of the other ‘switching’ applications. These constraints range from extreme modulation indexes to complex, unpredictable, and varying loads to bipolar, dual rail power supplies.

This study has captured the very few of these devices which do lend themselves to very efficient and very high-performance Audio Amplifier technologies.

From this study, it is apparent that there are a lot of trade-offs that are required in the optimization of the Class-D ‘switching’ Amplifier for the high-performance Audio application. Distortion is typically traded against Efficiency, which is traded against Noise Floor. At a much more detailed level, the desired or required voltage and current that are necessary to assure an accurate reproduction of the audio content start to affect these basic considerations. In the end, the design has to be manufacturable while not compromising the reliability, robustness, and performance of the product.

All of this considered, the GaN Systems technology and product offers the best possible system solution while not forcing compromises in quality and trade-offs of these device-level requirements.



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