GN002 Application Note

Thermal Design for GaN*PX*® Packaged Devices

GaN Systems Inc.

August 04, 2020

Application note outline

1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. Power loss and thermal modeling

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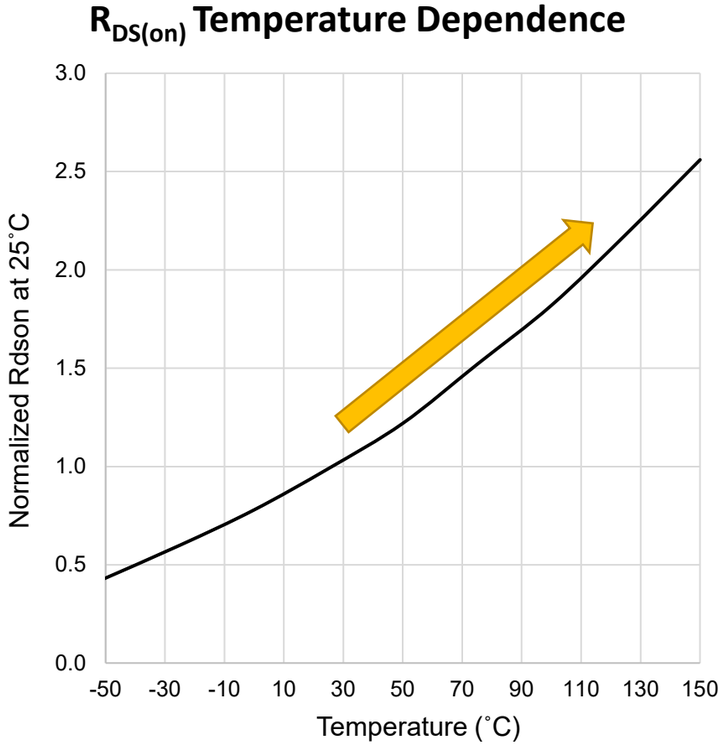
1. Motivation: device thermal management importance

Two electrical parameters that are dependent on temperature

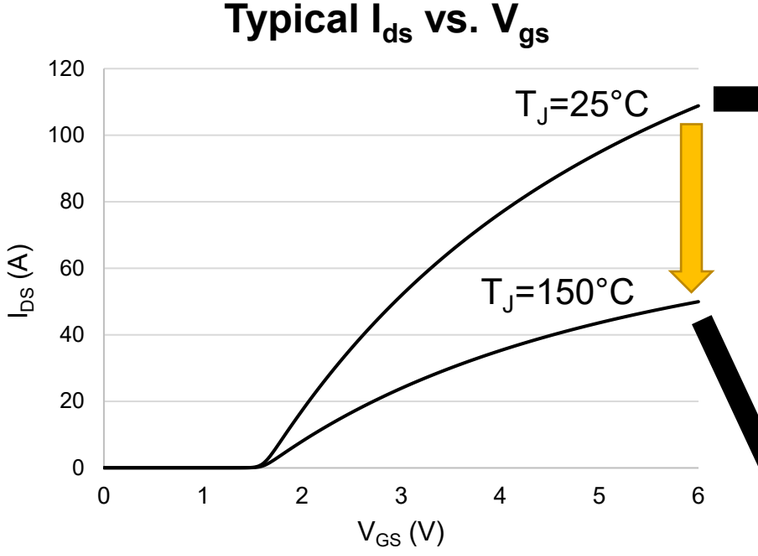
1. $R_{DS(on)}$ and conduction loss



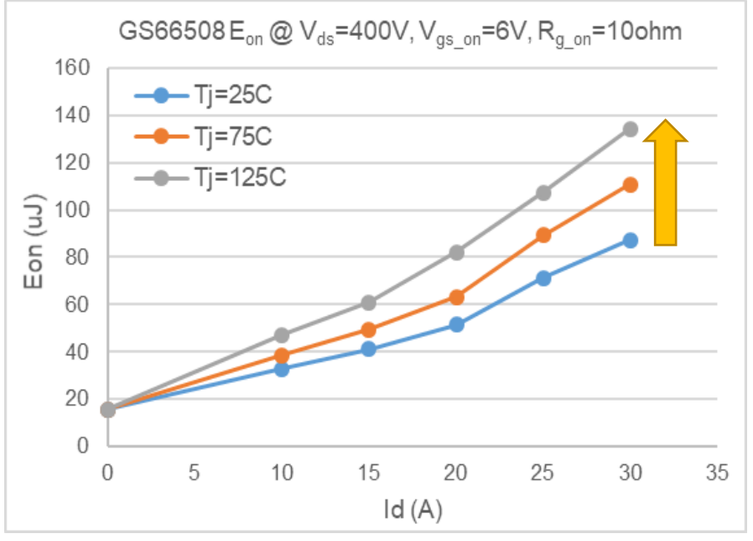
Rdson vs T_J for GS66508B

Need to properly manage T_J to minimize losses

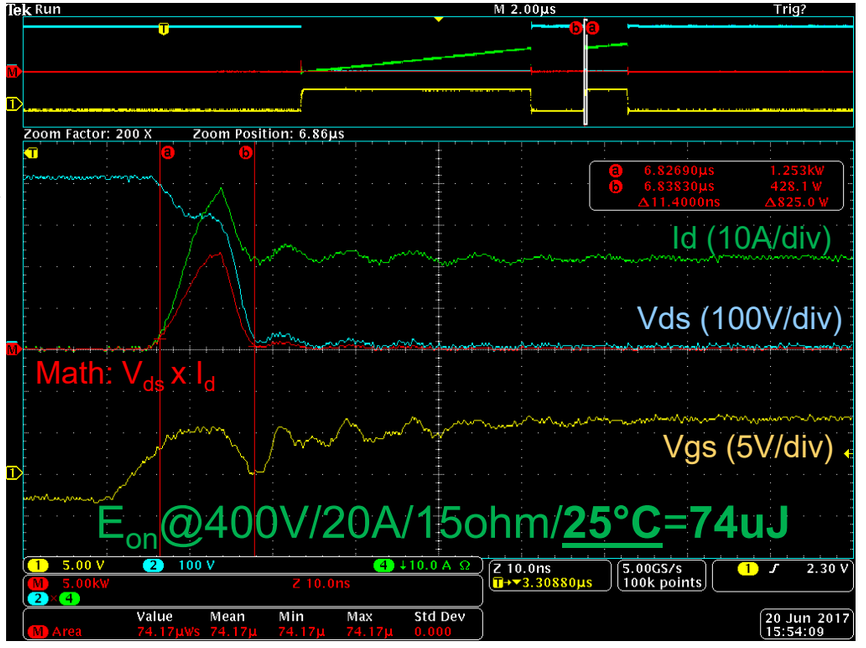
2. Transconductance and switching loss

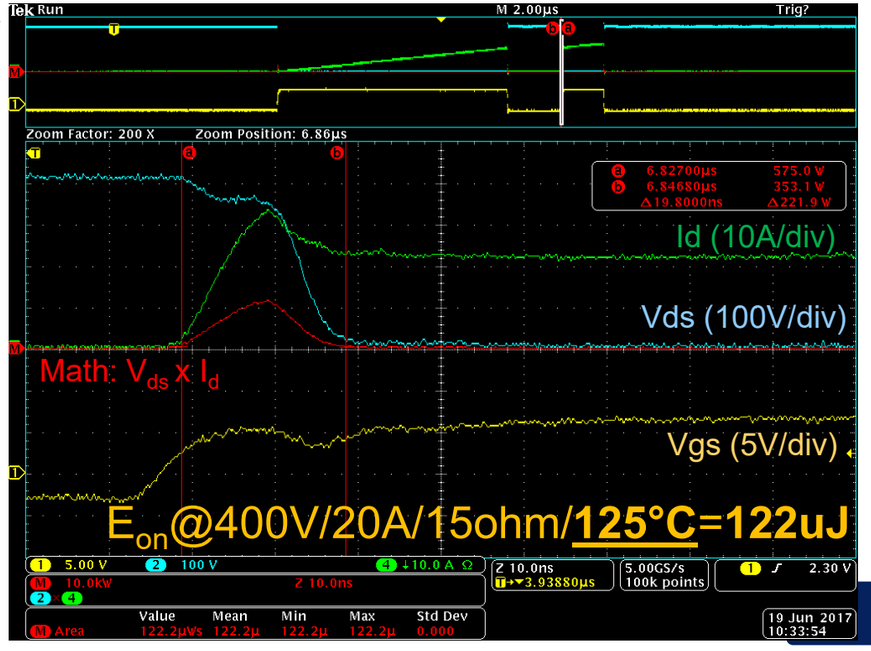


Transconductance g_m vs T_J for GS66508B



GS66508 E_{on} with T_J variation

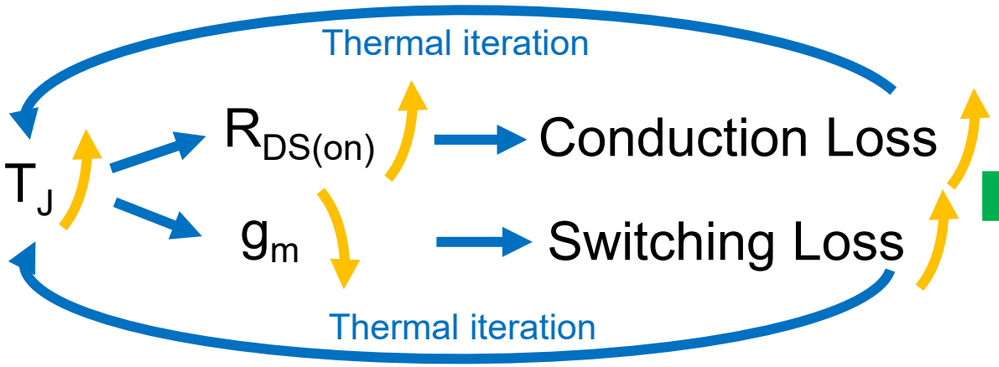




1. Motivation: device thermal management importance

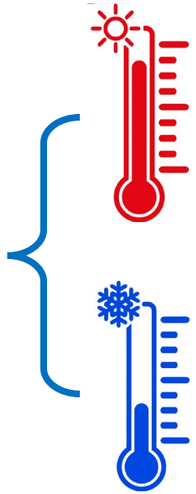
Reasons to keep device cool:

1. Prevents thermal runaway at maximum/worst operating conditions



Thermal runaway

Thermal steady-state



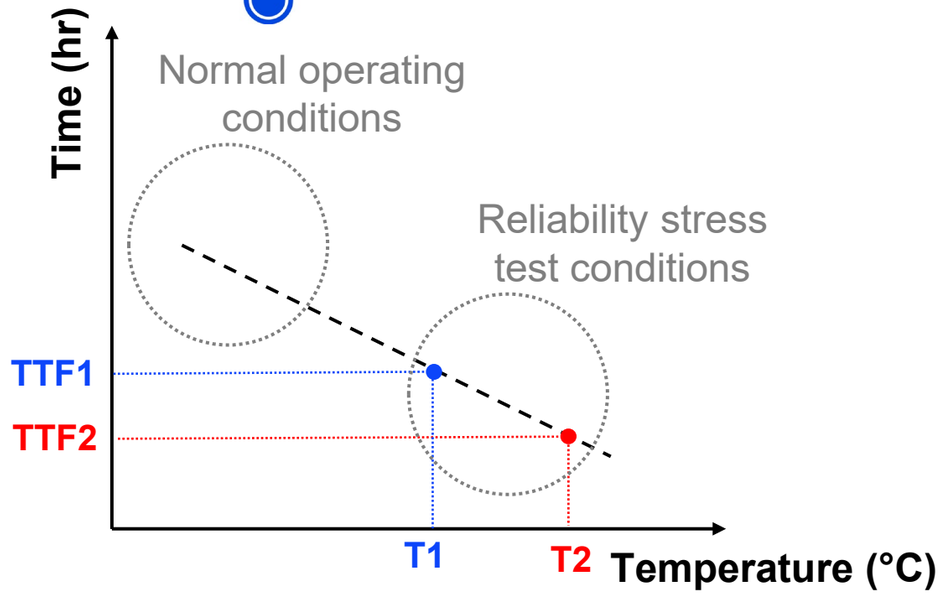
High junction temp T_J with **bad** thermal design

Low junction temp T_J with **good** thermal design

But also to:

2. **Reduce overall loss and improve system efficiency**
3. **Improve system reliability**

A good thermal design from both device-level and system-level is critical.



Time to failure with temperature acceleration

1. Motivation: device thermal management importance

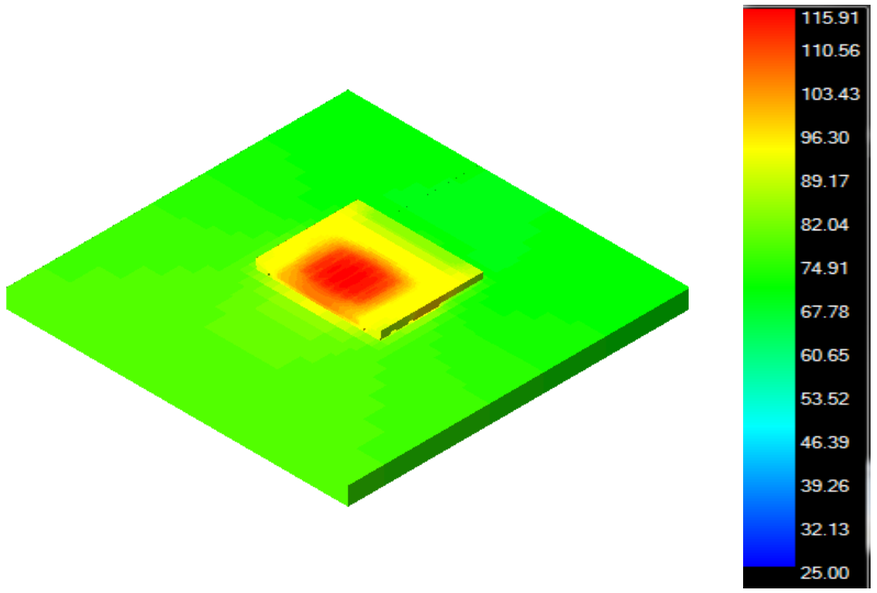
A good thermal design also improves design power density

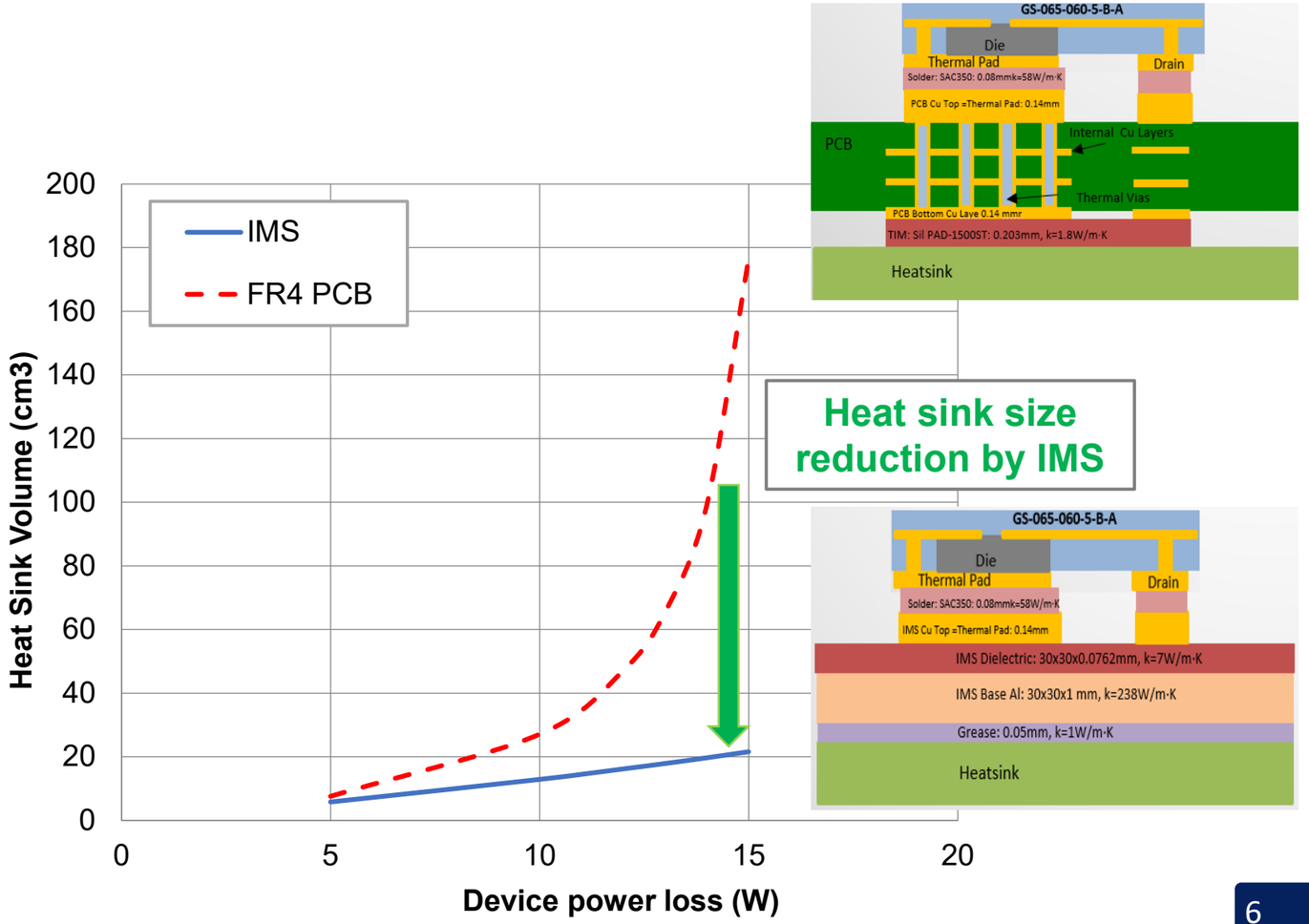
Example:

Compared to FR4 PCB heat transfer, the GaN Systems' insulated metal substrate (IMS) design reduces the heatsink volume for high-power applications

Simulation comparison of IMS vs FR4 PCB:

- Forced-air cooling, T_A=25 °C, same PCB size
- Keep T_J=100 °C. With power loss increasing, increase heatsink size to keep T_J constant.





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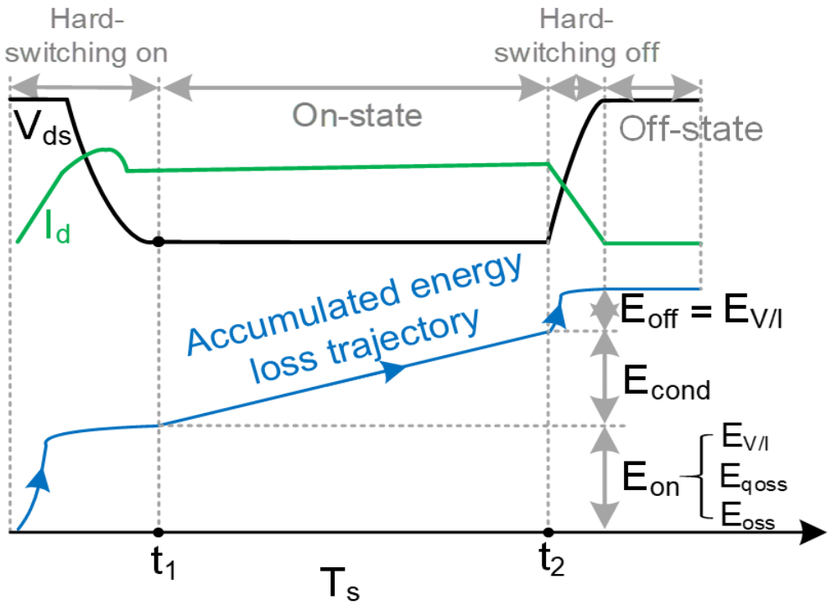
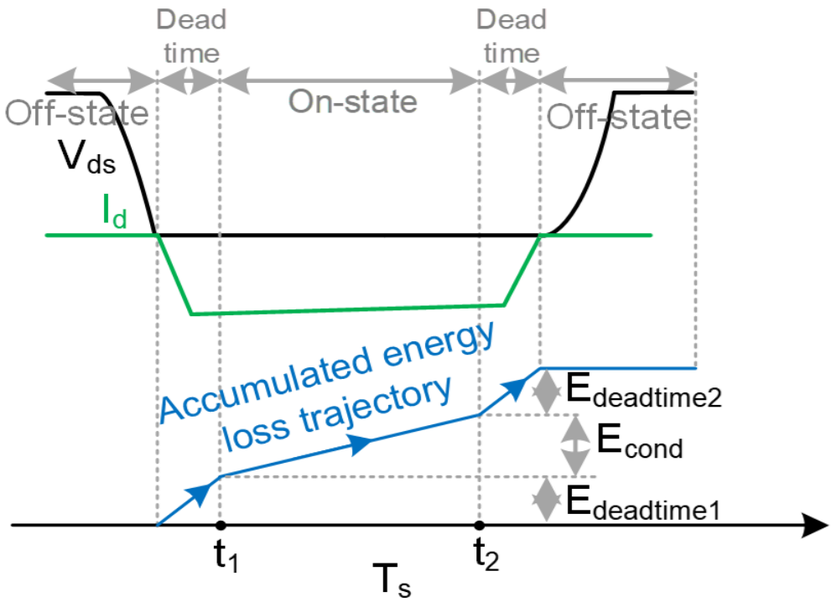
2. **Introduction of power loss and thermal basics**
    - 2.1 Power loss
    - 2.2 Heat transfer, thermal resistance, and junction temperature
3. Bottom-cooled device thermal design consideration
4. Top-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. Loss and thermal modeling

2.1 Introduction of power loss mechanism

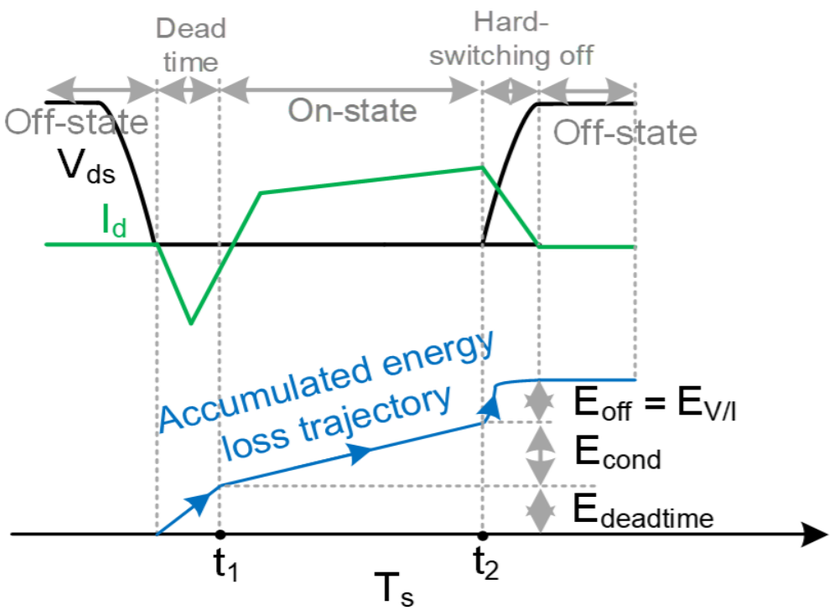
Switch device's energy loss can be mainly summarized as three different types. Power loss is $P = E \times F_{sw}$



1. Hard-switching device energy loss trajectory

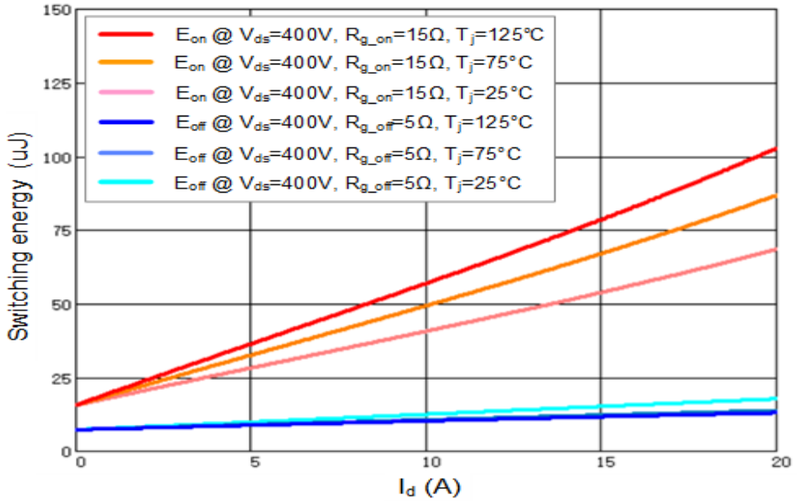


2. Synchronous-rectification device energy loss trajectory

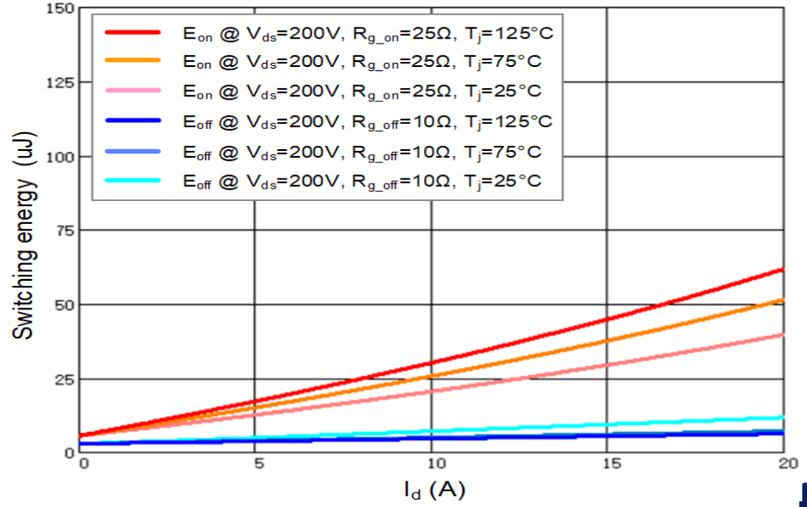


3. ZVS soft-switching device energy loss trajectory

Power loss mechanisms under various operating conditions are well understood and characterized



GS66508T switching loss @ 400V

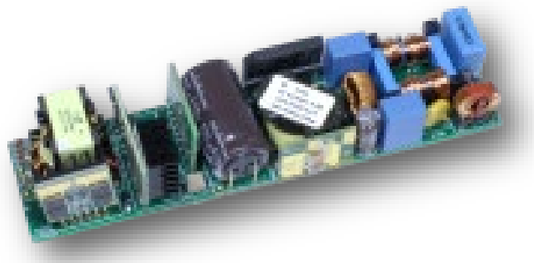


GS66508T switching loss @ 200V

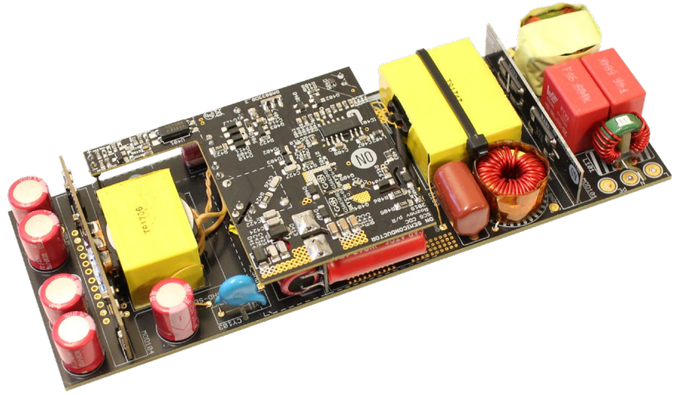
2.1 Introduction of power loss reduction by using GaN

Switching method	GaN characteristics	System impact
3. ZVS soft-switching mode	Fast switching speed	Switching-off loss ↓
	Low energy-related $C_{oss(ER)}$	Inductive energy to achieve ZVS, less reactive power loss ↓
	Low time-related $C_{oss(TR)}$	Deadtime ↓
	Low gate charge Q_g	Gate driver loss ↓
1. Hard-switching mode	Zero reverse recovery loss Low capacitive E_{oss}/E_{qoss} loss Excellent transconductance	Switching-on loss ↓

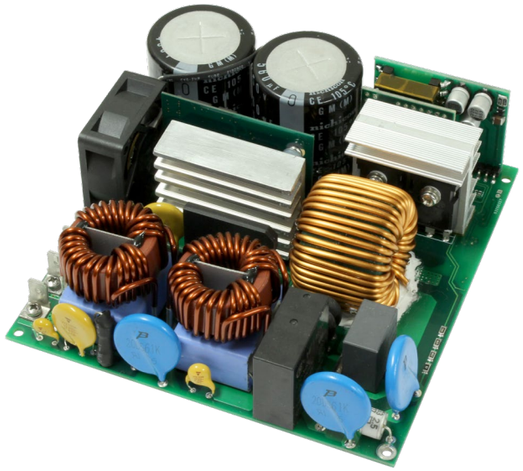
Due to its excellent electrical performance, GaN HEMT enhances both soft-switching and hard-switching applications



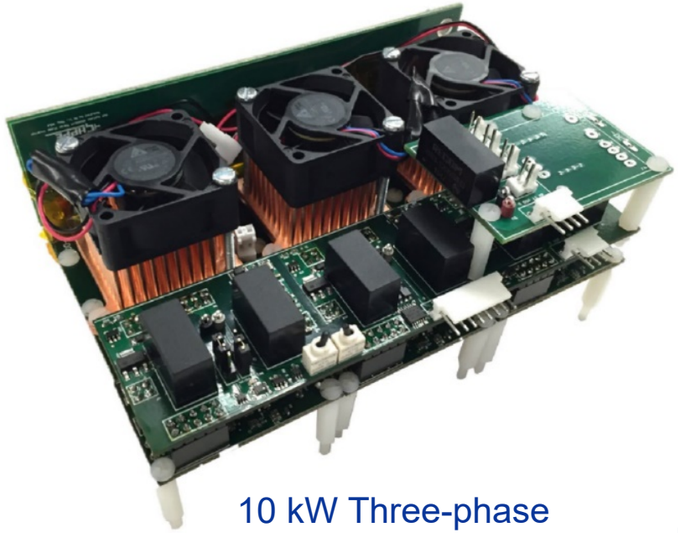
170 W PFC + LLC adapter



300 W PFC + LLC adapter



3 kW CCM Totem-pole PFC

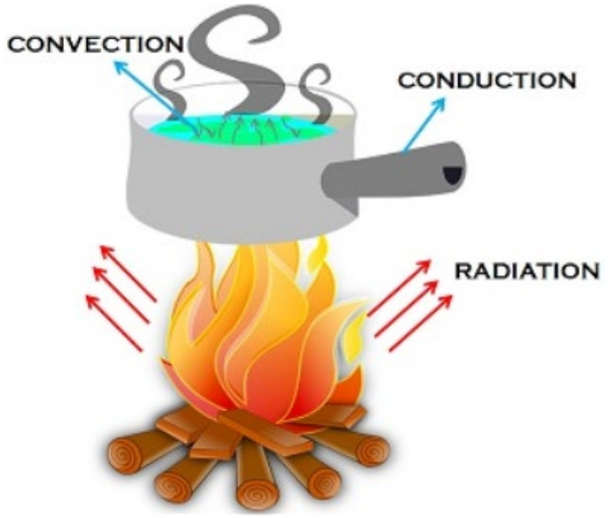


10 kW Three-phase traction inverter

2.2. Heat transfer, thermal resistance, and junction temperature

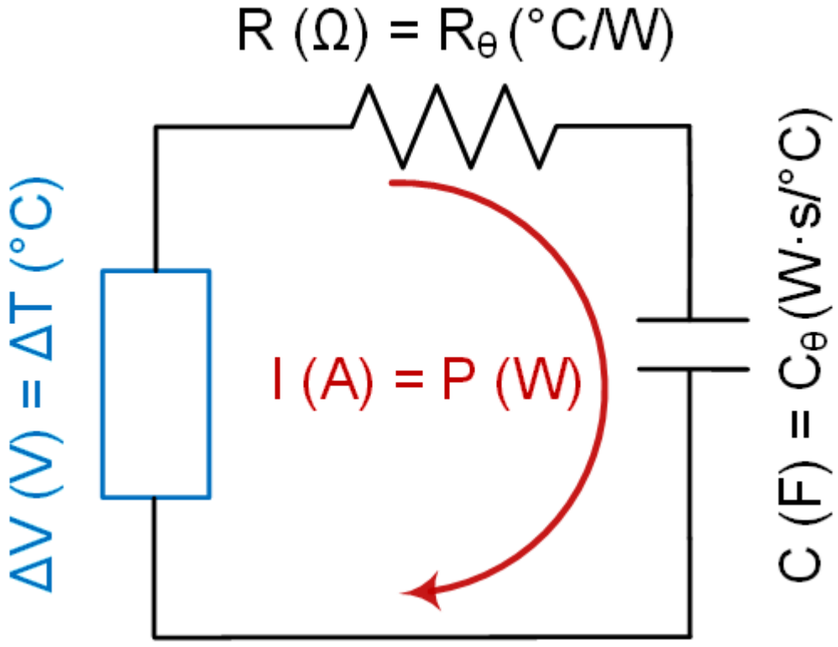
Heat transfer occurs mainly in three different ways:

- **Conduction** – through direct contact
- **Convection** – through fluid movement (air is a fluid)
- **Radiation** – through electromagnetic waves

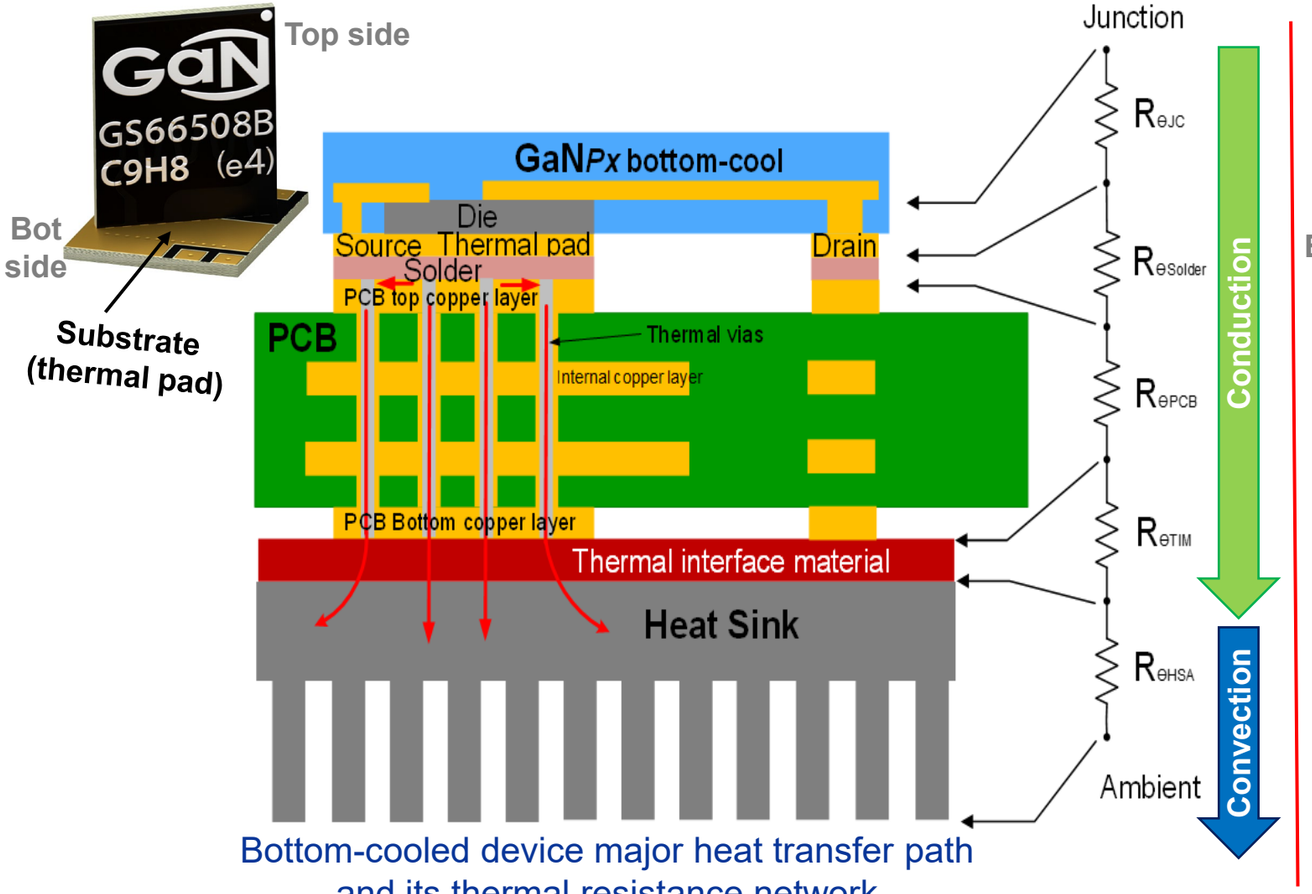


Analogy between thermal and electrical parameters

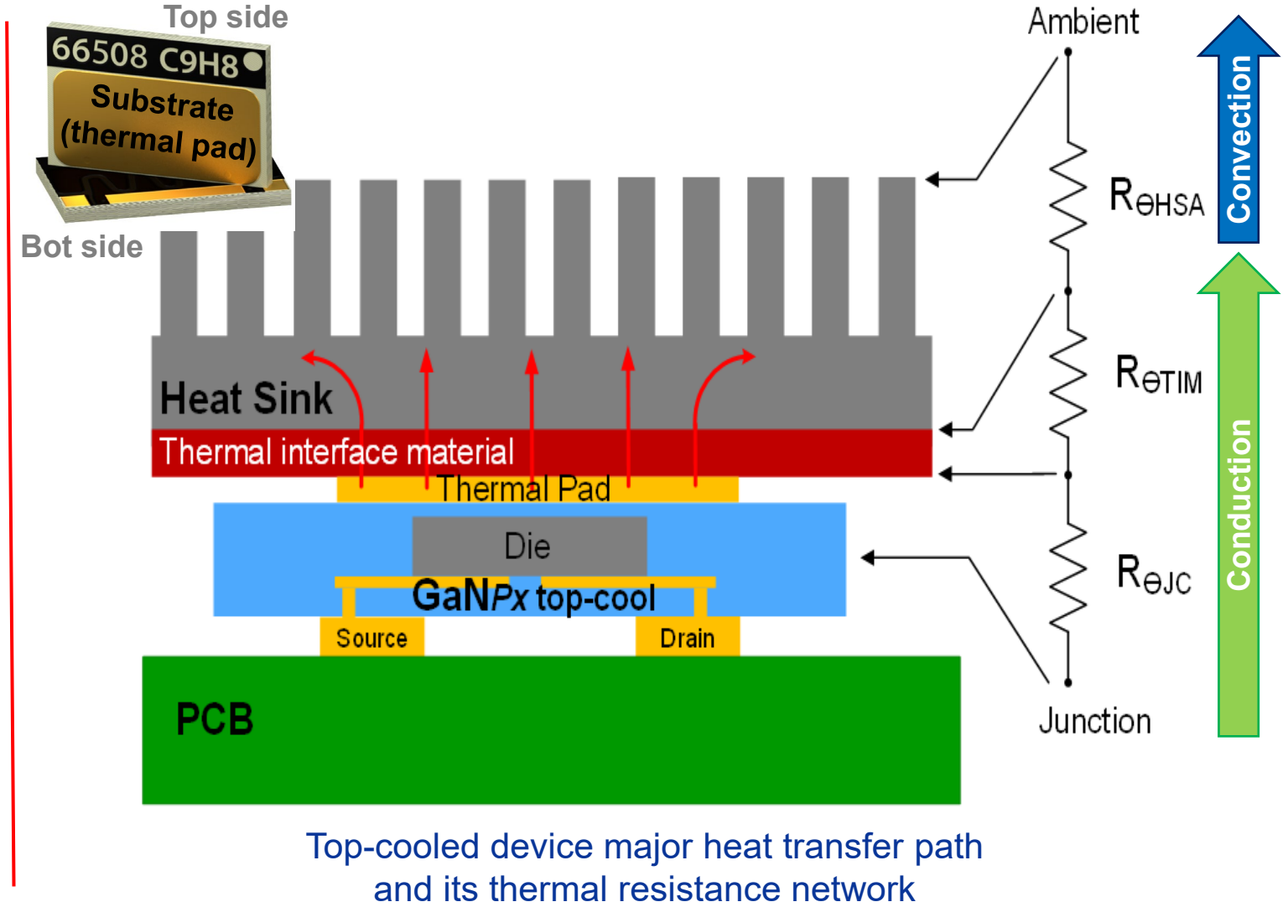
Thermal parameters	Electrical parameters
Temperature T (°C)	Voltage V (V)
Power P (W)	Current I (A)
Thermal resistance: R_θ (°C/W)	Resistance R (Ω)
Thermal capacitance: C_θ (W·s/°C)	Capacitance C (F)



2.2. Heat transfer and thermal resistance on GaN



Bottom-cooled device major heat transfer path and its thermal resistance network



Top-cooled device major heat transfer path and its thermal resistance network

Junction temperature calculation: $T_J = T_A + P \times R_{\theta JA}$

Excellent electrical performance (figure-of-merit) of GaN HEMTs limit the overall power loss

Beyond conventional "figure-of-merit"
This presentation shows how to fully utilize GaN by thermal design to maximize the overall performance of GaN HEMTs

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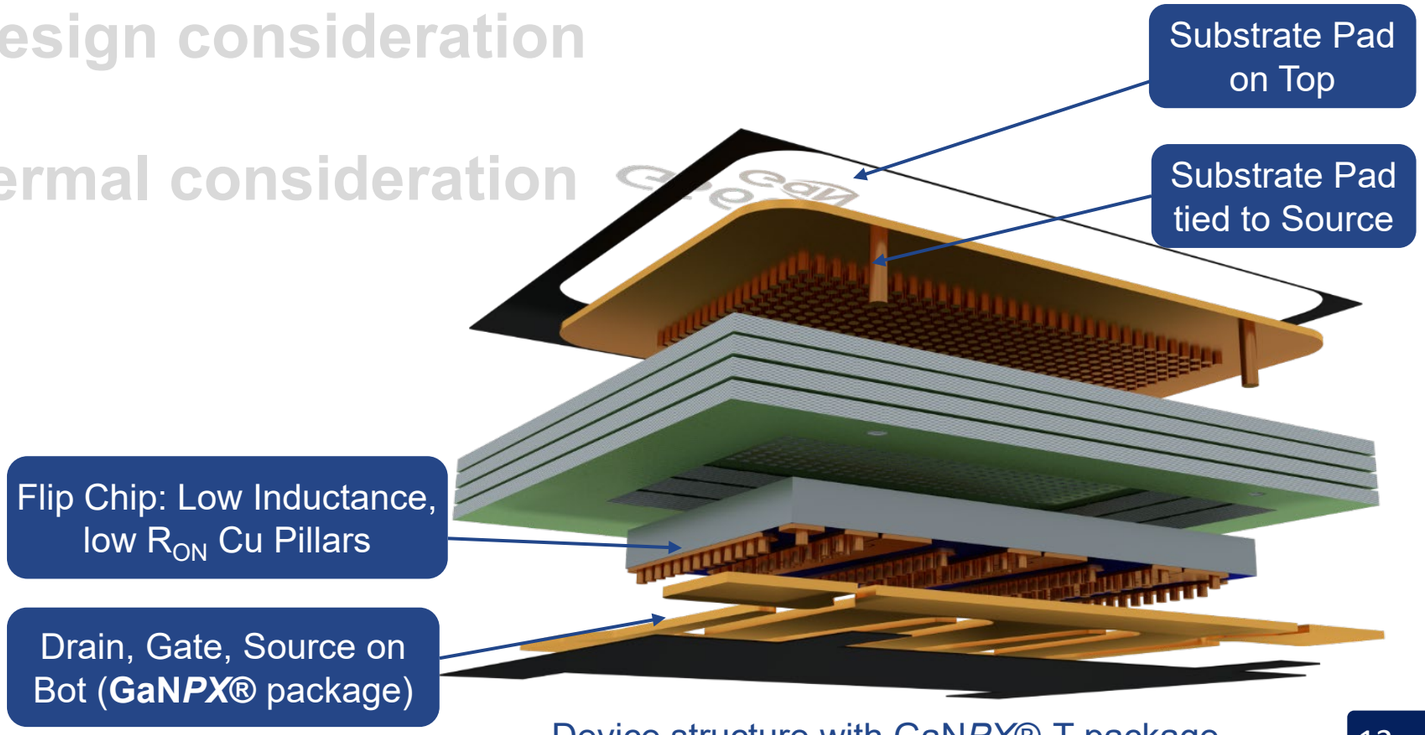
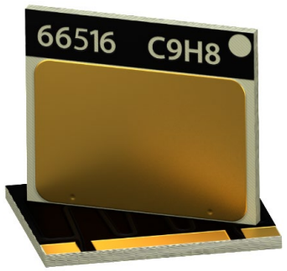


Device structure with GaN*PX*®-T package

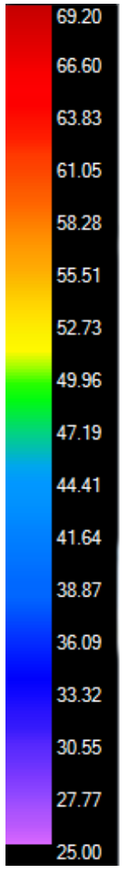
3. Top-cool design – Thermal interface material (TIM) selection

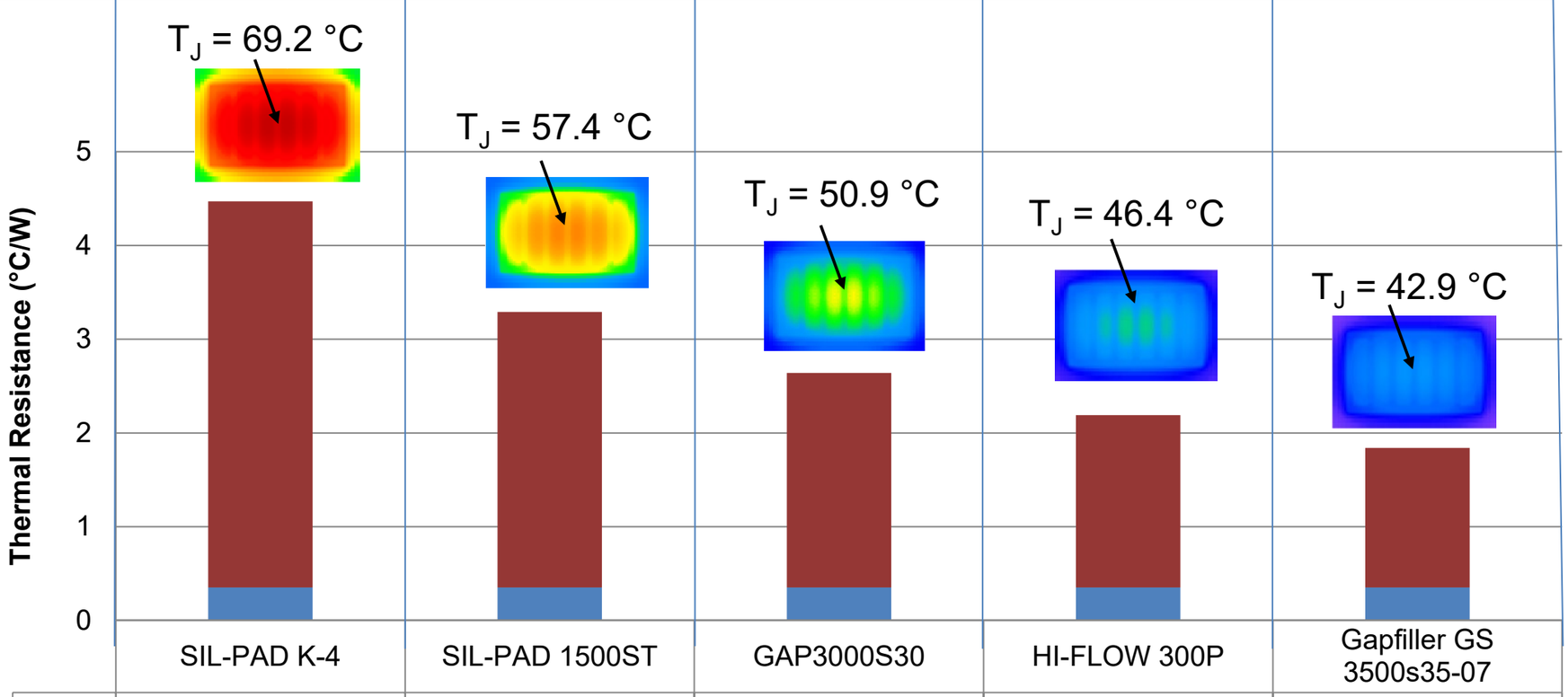
Thermal simulation operating Conditions:

- GS66516T is applied with 10 W power loss on it
- T_{HS} = 25 °C



	SIL-PAD K-4	SIL-PAD 1500ST	GAP3000S30	HI-FLOW 300P	GAPFILLER GS 3500S35-07
TIM Thickness (mm)	0.152	0.203	0.25	0.102	0.178
Thermal conductivity (W/m·K)	0.9	1.8	3.0	1.6	3.6





	SIL-PAD K-4	SIL-PAD 1500ST	GAP3000S30	HI-FLOW 300P	Gapfiller GS 3500s35-07
RTIM	4.12	2.94	2.29	1.84	1.49
RJC	0.35	0.35	0.35	0.35	0.35

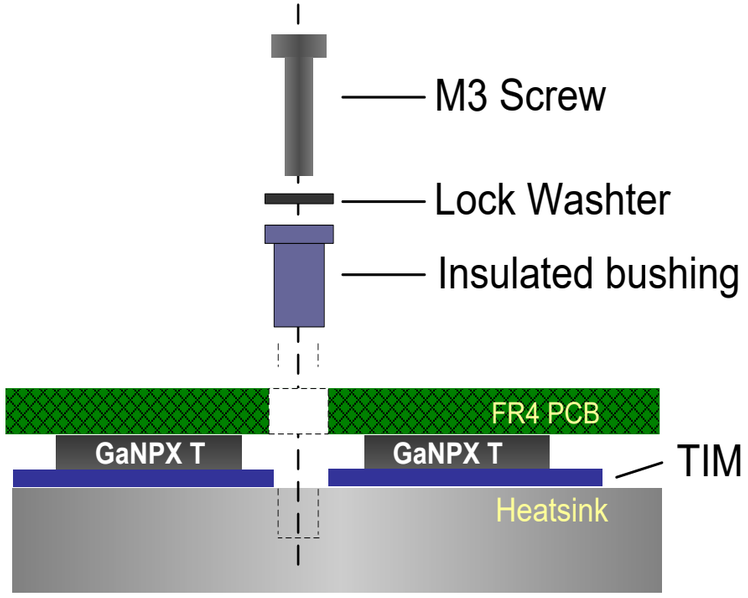
Key parameters for TIM material selection: dielectric strength, mechanical strength, and cost.

Listed TIM materials from Bergquist *http://www.bergquistcompany.com/thermal_materials/

3. Top-cool design – Mounting consideration

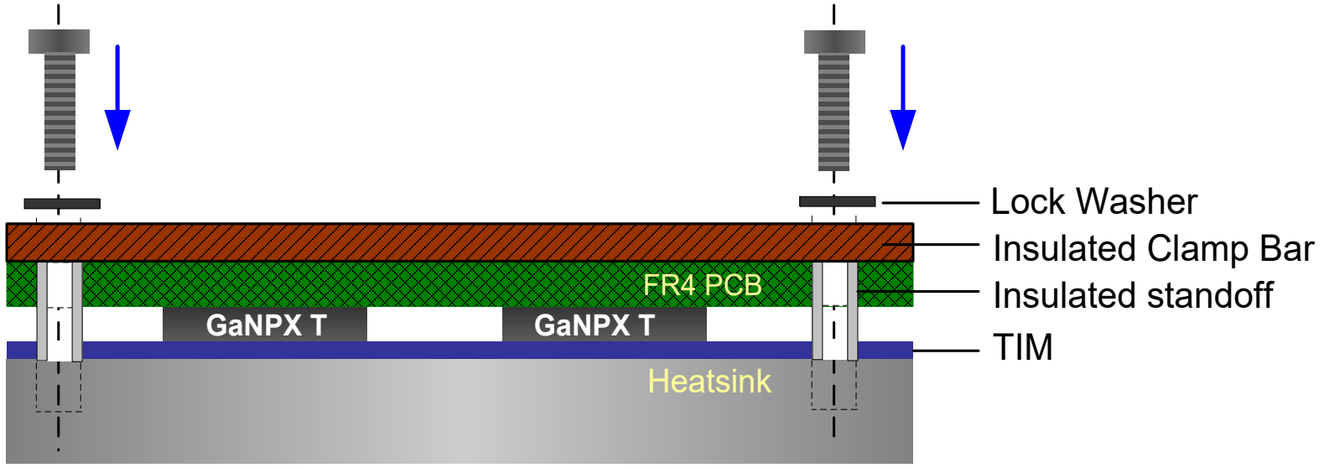
Center mounting hole for small heatsink

- Balanced pressure across 2 devices
- Typical recommended maximum pressure ~50psi.
- Tested up to 100psi without failure



2 or more mounting holes for large heatsink

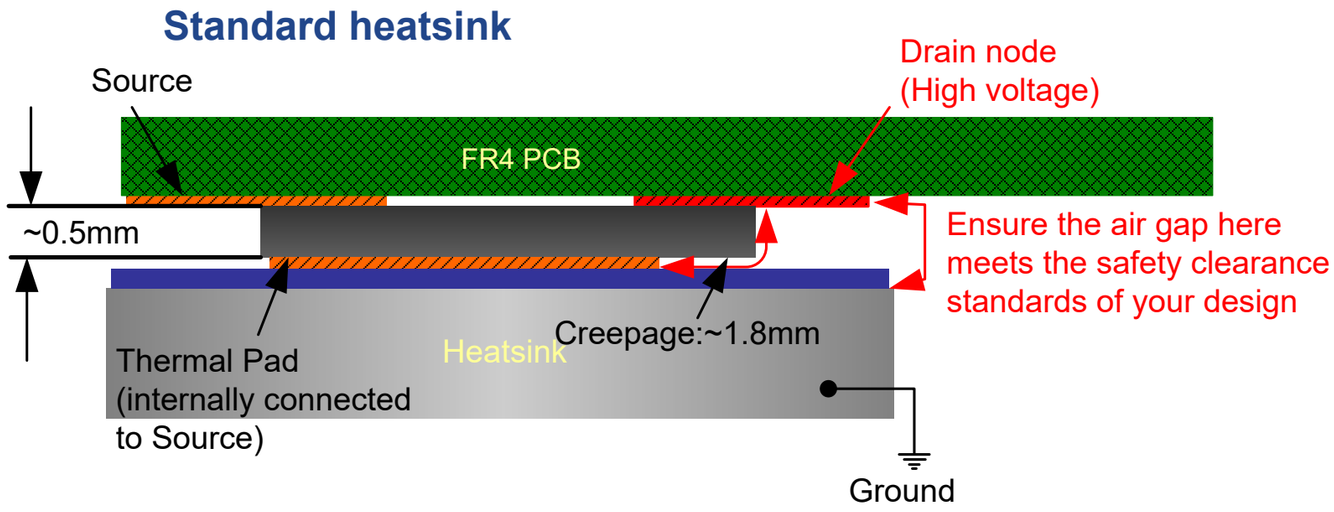
- Excess PCB bending causes stress on SMD parts which should be avoided
- Locate mounting holes near to GaN*PX*®-T package
- If warranted, use a supporting clamp bar on top of PCB for additional mechanical support, not common

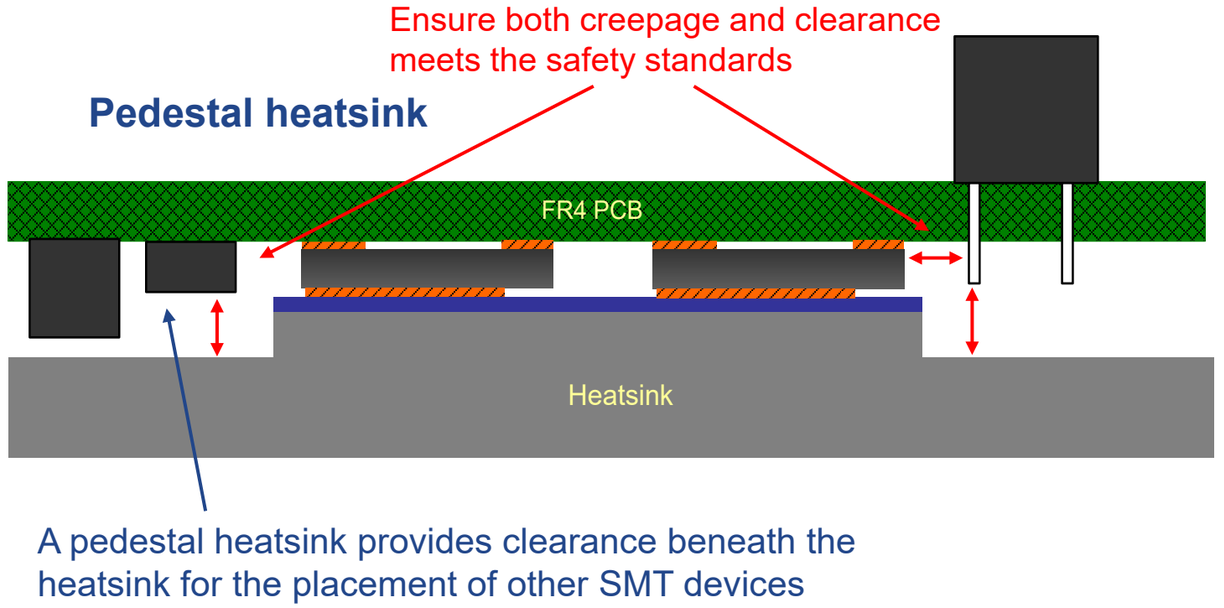


3. Top-cool design – Voltage isolation clearance

When using a heatsink, design to meet the regulatory creepage and clearance requirements

- Use TIM to cover Heatsink edge in areas where clearances must meet Standards
- Avoid placing Through Hole Components near GaN*PX*® -T package
- Use **Pedestal Heatsink** design to increase clearances and allow for placement of SMT components under the heatsink

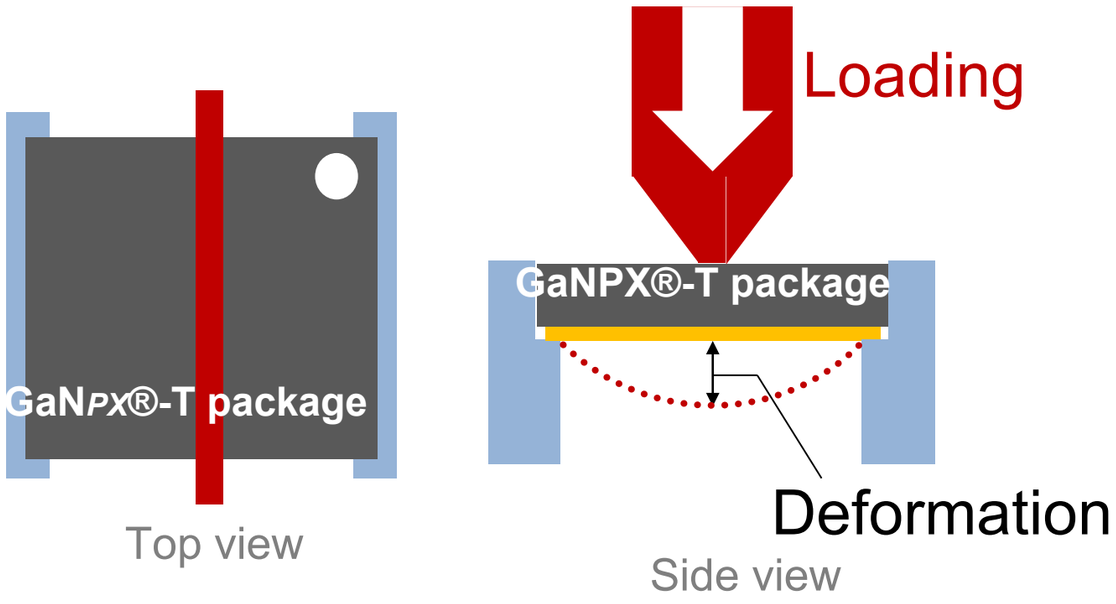




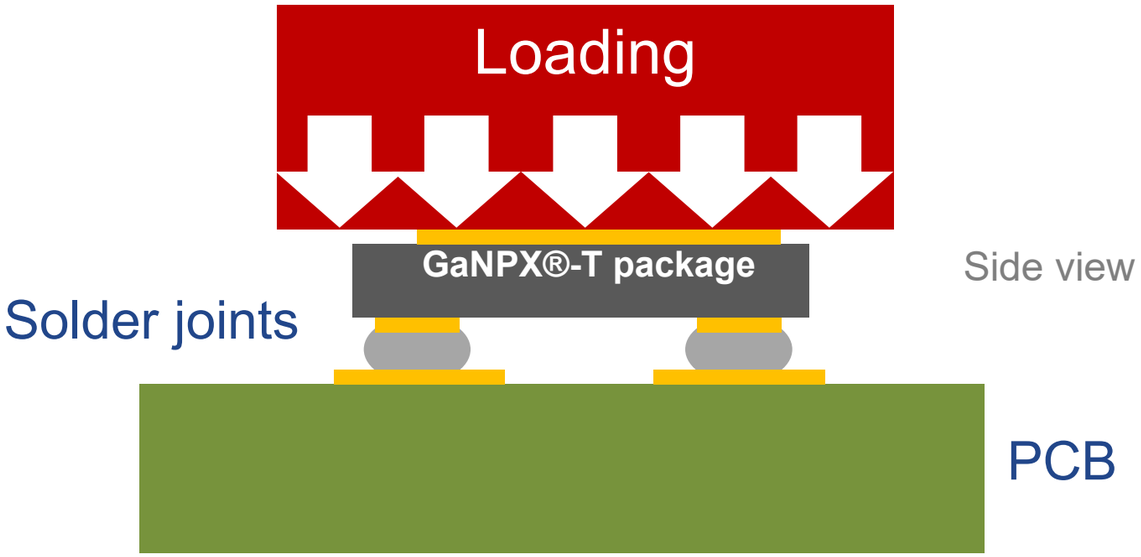
3. Top-cool design – Package bending pressure and deformation

Part Number	Deformation Safe Limit (µm)	Pressure Safe Limit (PSI)
GS66508T	50	100
GS66516T	120	100

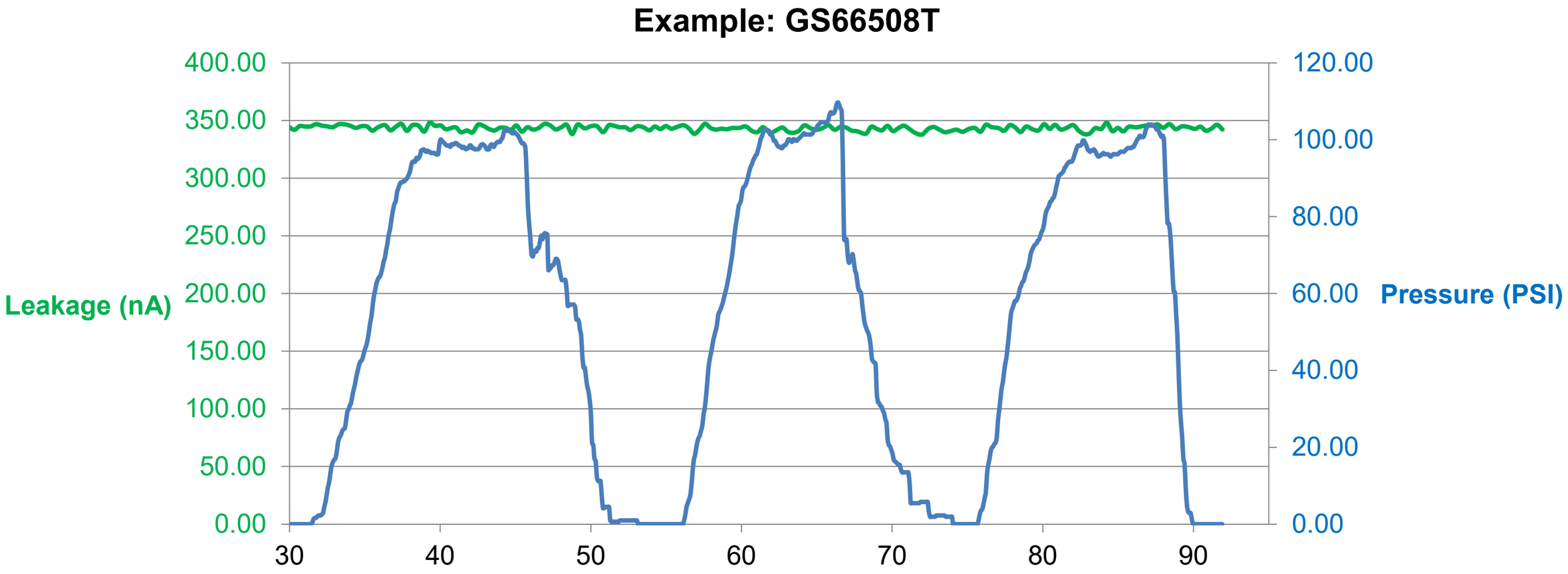
Deformation Test



Pressure Test



3. Top-cool design – Bending Pressure Test Methodology



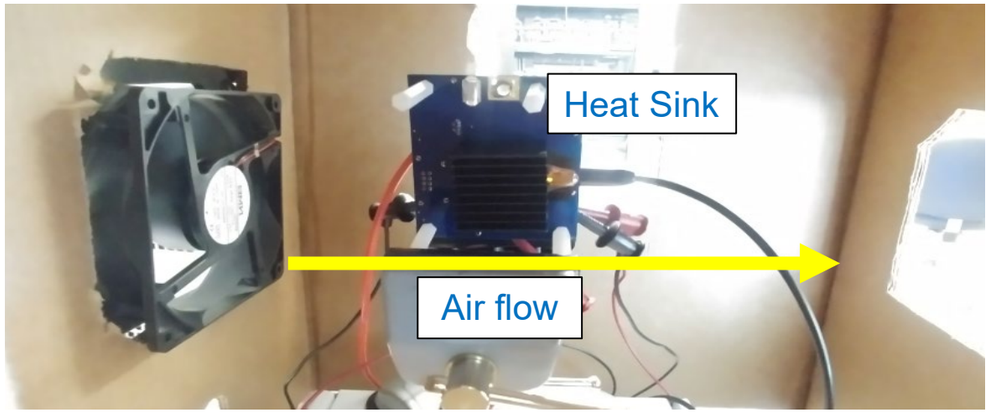
DUT subject to 100 PSI over 3 pulses, with no shift in Leakage Currents

400 volts V_{DS} applied to each DUT (@ 25˚C)

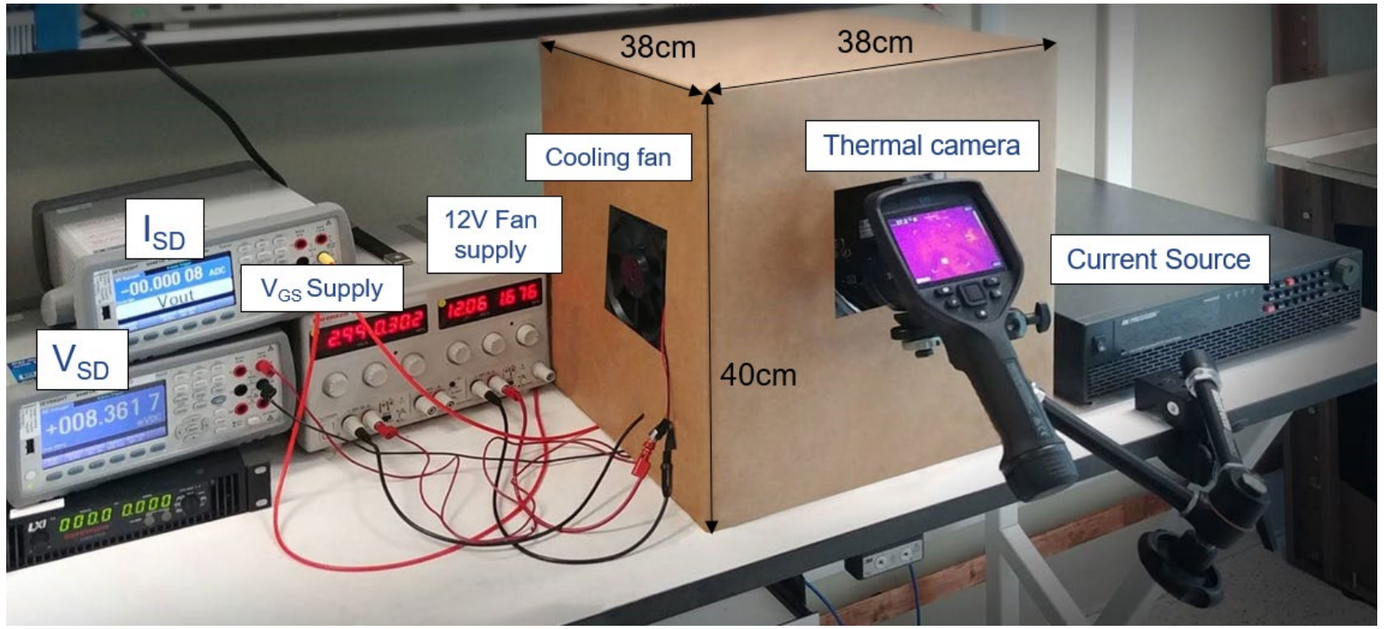
Leakage Current = I_{DSS} + I_{GS} + I_{BULK}* (*Substrate)

3. Top-cool design – Thermal resistance measurement

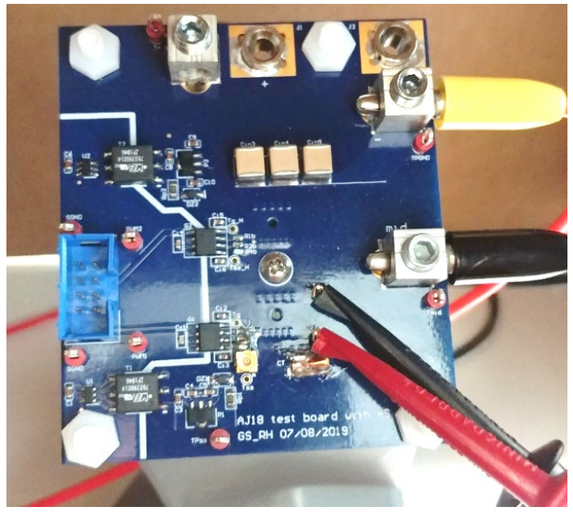
1. The measured $R_{\theta JHS}$ and $R_{\theta JA}$ for GS66516T are 3 °C/W and 4.2 °C/W, respectively.
2. GS66516T can dissipate 29 W loss per device.



Inside setup box region



Top-cool force-air cooling thermal Resistance test setup

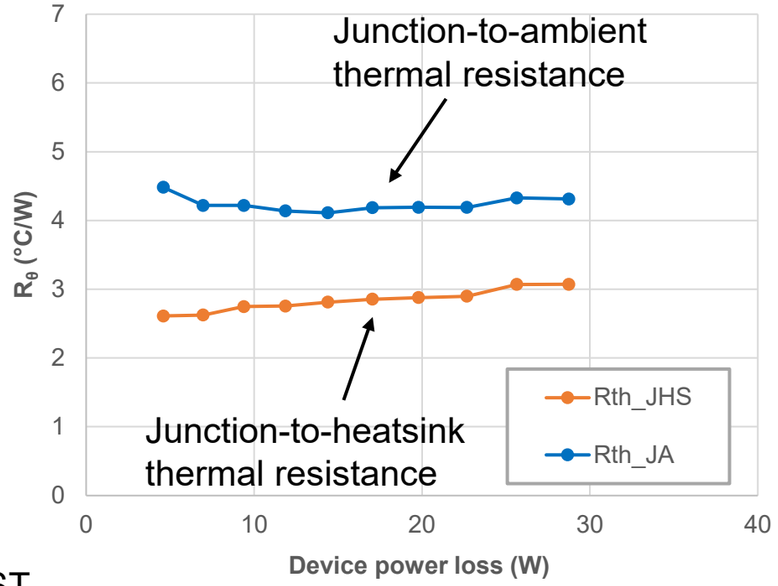


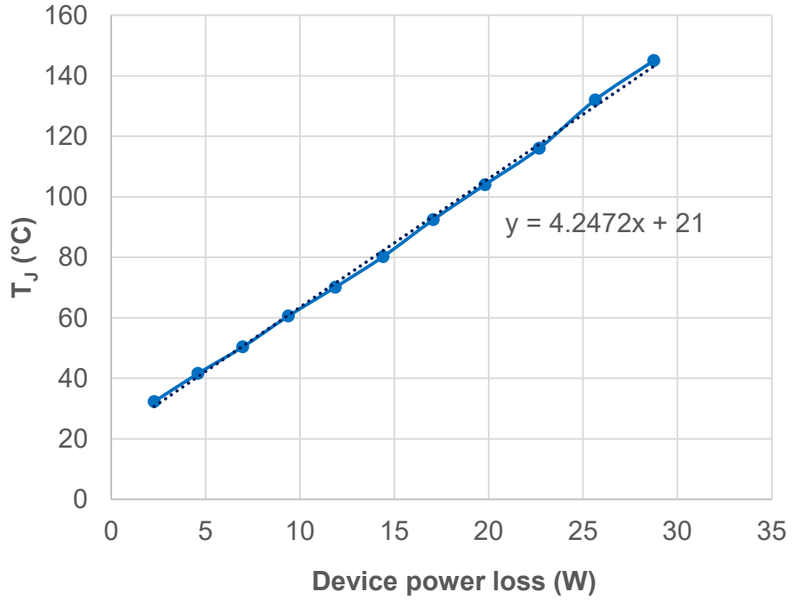
Tested GS66516T-based evaluation board

Heat sink size: 3.4x3.4x2.5 cm^3

Fan flow rate: 3.3 m^3/min

TIM: Sil-Pad 1500ST





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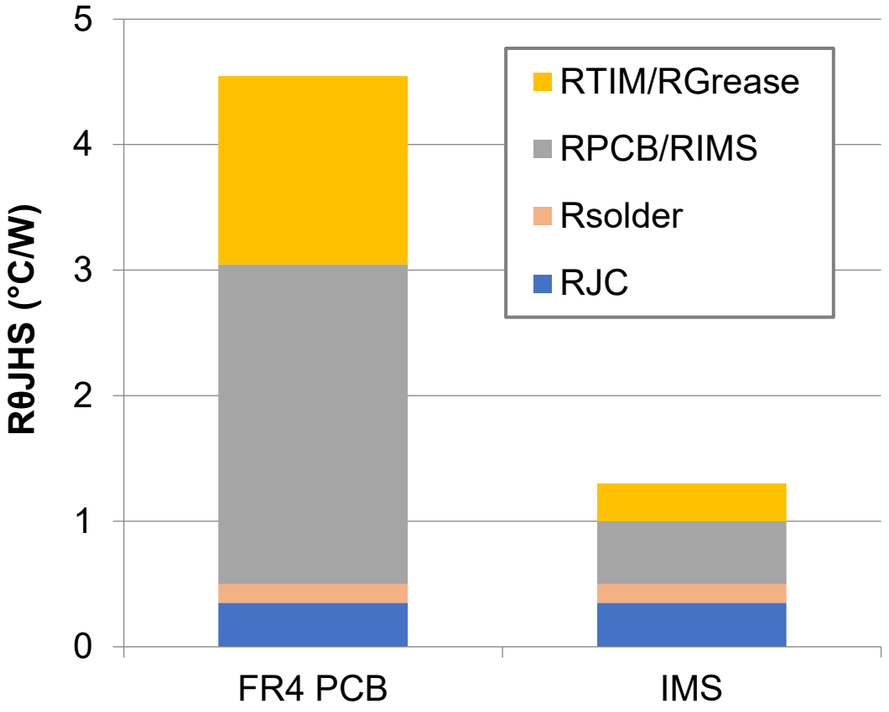
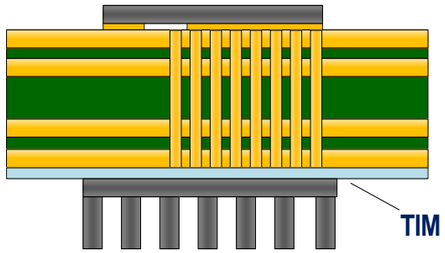
    - 4.1 FR4 PCB Bottom-cool design
    - 4.2 IMS Bottom-cool design
5. Device selection based upon thermal consideration
6. Loss and thermal modeling

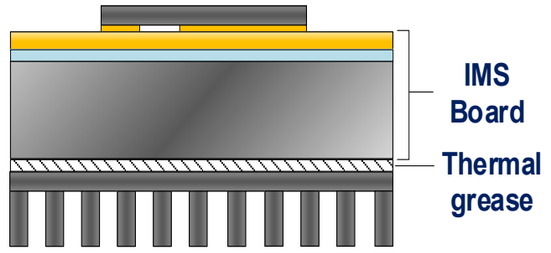
4. Bottom-cooled device thermal design

Bottom-cooled device thermal solutions summary



Comparison of junction-to-heatsink thermal resistance ($R_{\theta JHS}$) based on GS66516B





	FR4 PCB Cooling with Vias	Insulated Metal Substrate (IMS)
Thermal resistance	Good	Best
Electrical Insulation	Use TIM	Yes
Cost	Lowest	Low
Advantages	• Standard process • Layout flexibility	• Electrically isolated
Design challenges	• High PCB thermal resistance	• Usually layout limited to 1 layer • Parasitic inductance • Coupling capacitances to the metal substrate

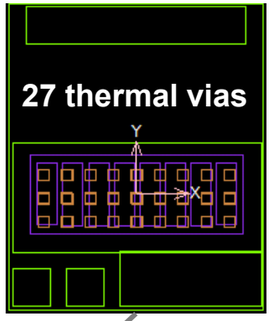
Performance comparison of 2 thermal design options for bottom-cool devices

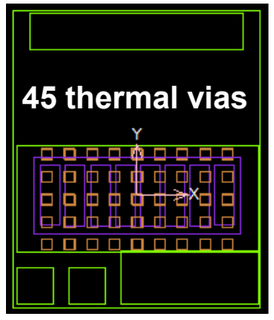
FR4 PCB and IMS for bottom-cooling are both suitable solutions. Customer selection depends on design trade-off

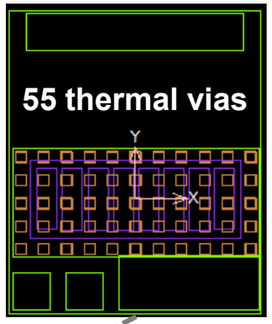
4.1. FR4 PCB Bottom-cool design – PCB thermal design

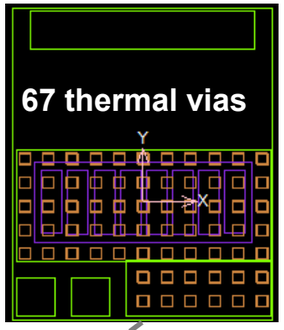
Thermal vias design

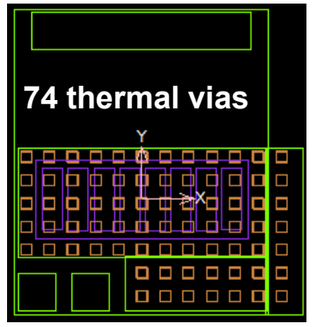
- GS66508B with device power loss 10 W. 4 layers copper with 2 oz (70 µm) copper thickness. T_{HS} = 25 °C
- Thermal via setup:0.3 mm diameter with 0.64 mm pitch. Standard 25 µm copper plating thickness. No via filling.

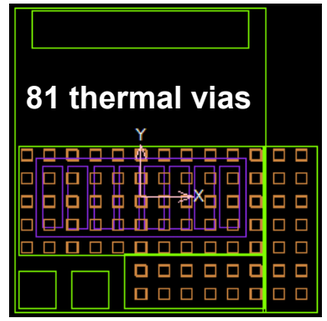


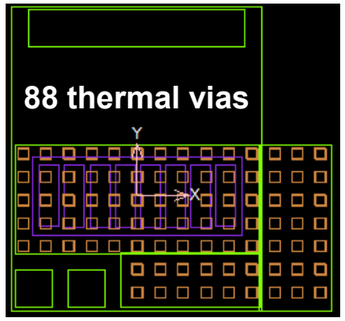


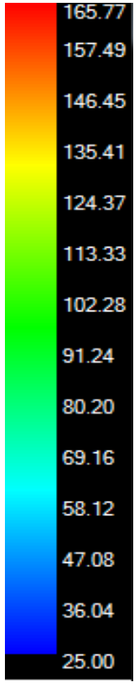




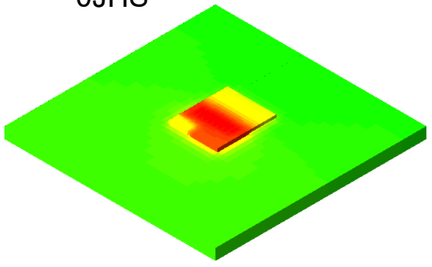






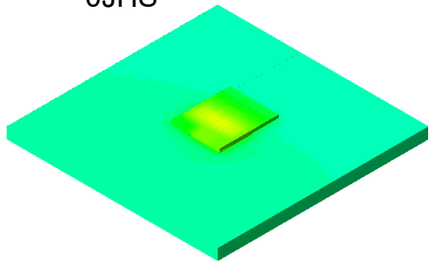


$R_{\theta JHS}$ = 14.1 °C/W



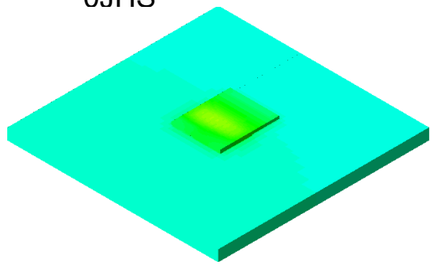
27 Thermal Vias

$R_{\theta JHS}$ = 8.8 °C/W

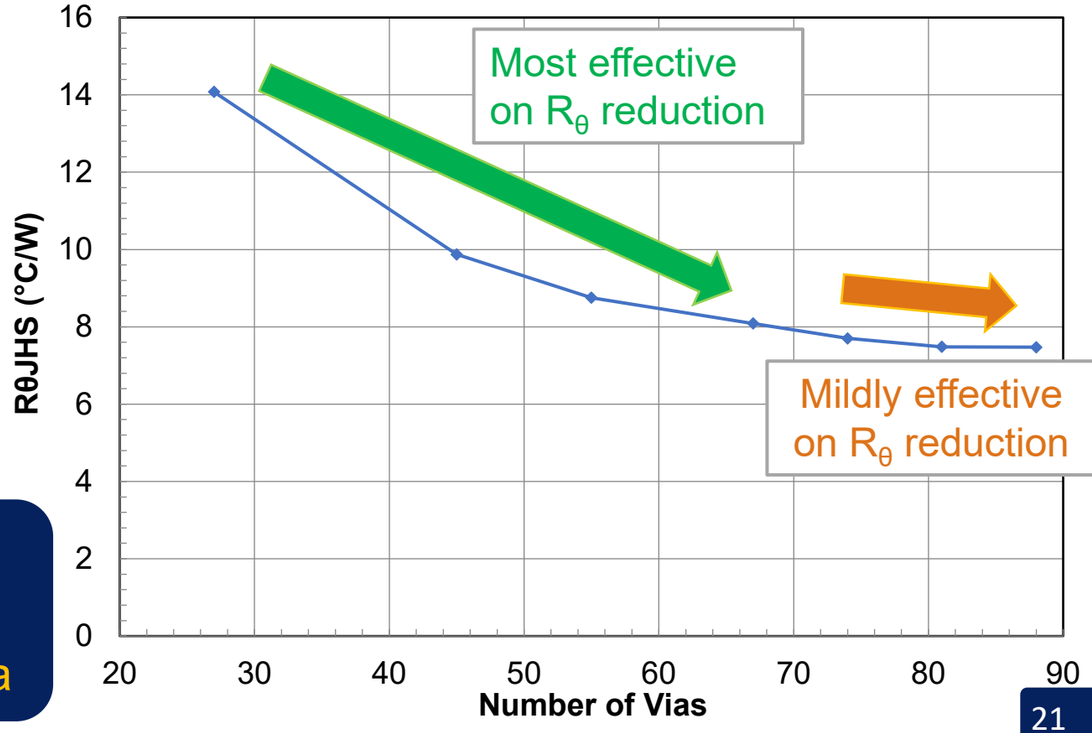


55 Thermal Vias

$R_{\theta JHS}$ = 8.1 °C/W



67 Thermal Vias

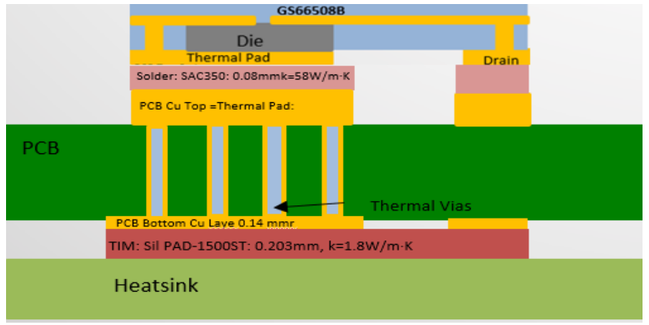


- Place thermal vias fully under the device thermal pad to maximize effectiveness
- Thermal via area is extendable based upon PCB design area

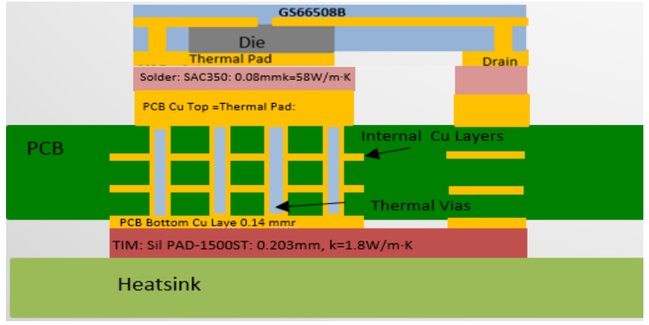
4.1. FR4 PCB Bottom-cool design – PCB thermal design

Number of copper layers and copper thickness

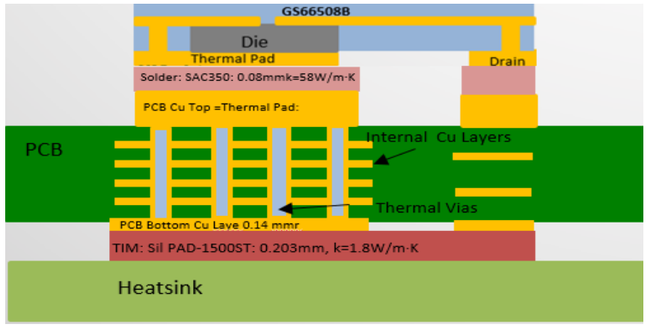
- GS66508B with device power loss 10 W. T_{HS} = 25 °C. Overall PCB thickness keeps the same (1.6mm).
- With 55 thermal vias as example.



2 layer PCB design

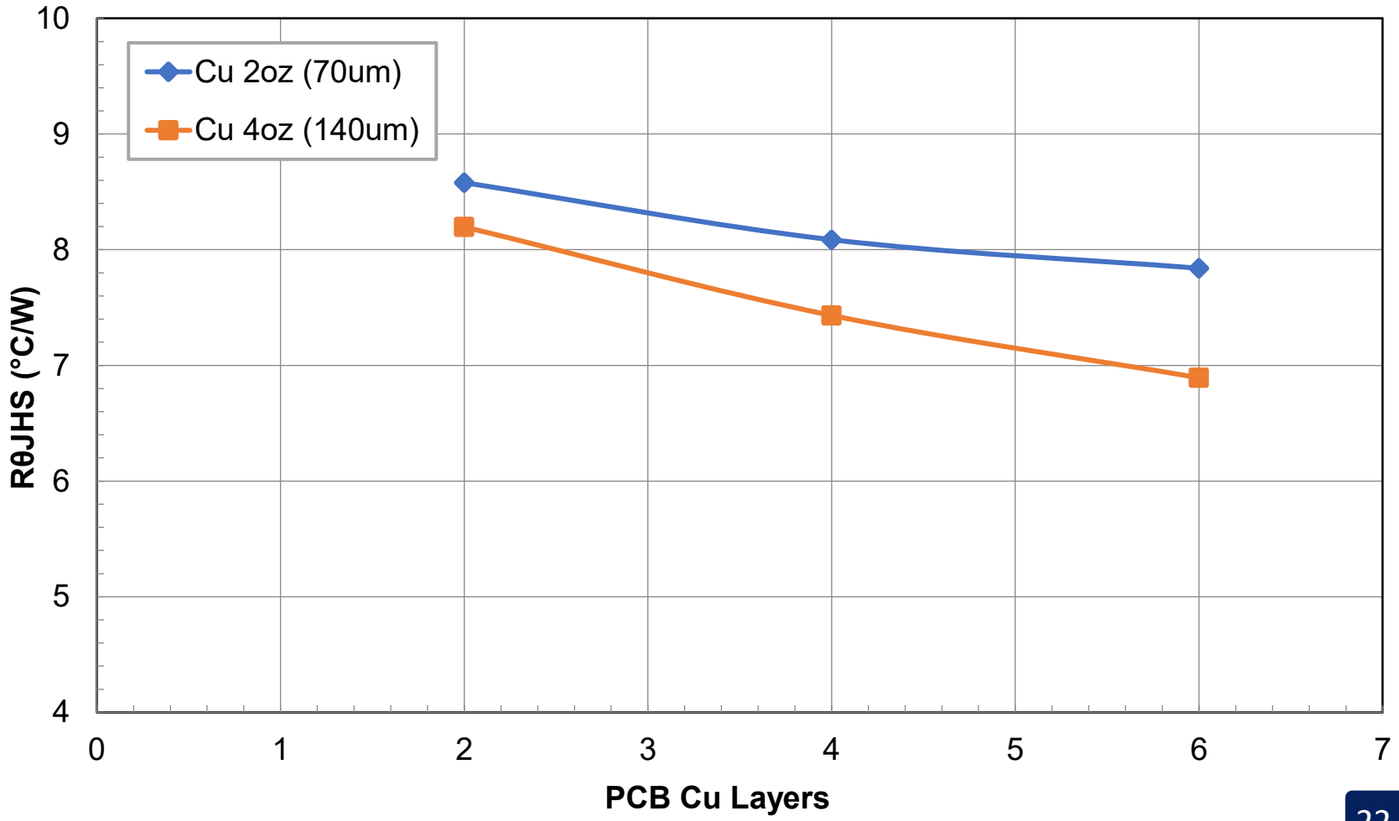


4 layer PCB design



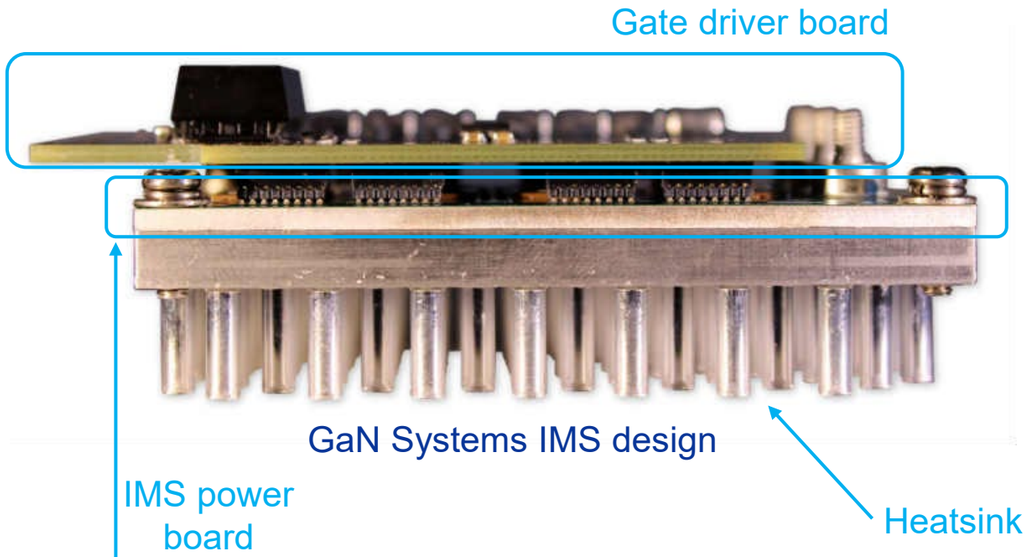
6 layer PCB design

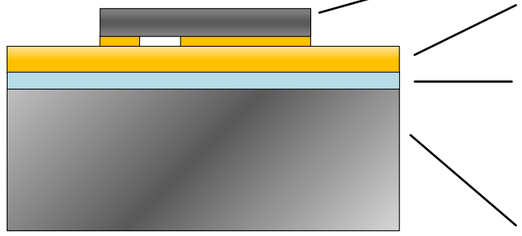
Increase in copper layer and copper thickness reduces R_θ further, with the PCB cost as the trade-off



4.2. IMS Bottom-cool design

Cross section view of IMS design





SMT Power Package

Copper Foil:
- Typ. 1-4oz (35-140um) up to 10oz

Dielectric Layer:
- Electrical insulation
- Typ. 30-200um thickness
- Thermal conductivity: 1-3W/mK

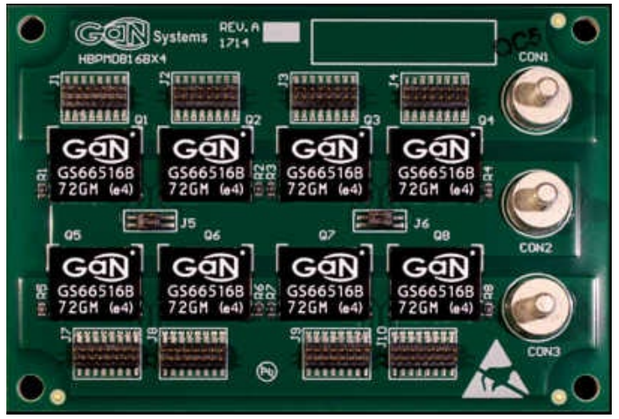
Metal Substrate/Base
- Electrically isolated
- Aluminum or copper

IMS improves power density for high-power applications

IMS I

- Designed for high power application (3~12kW).
- Applied GaN HEMT: GS66516B single, or 2x, 4x paralleling

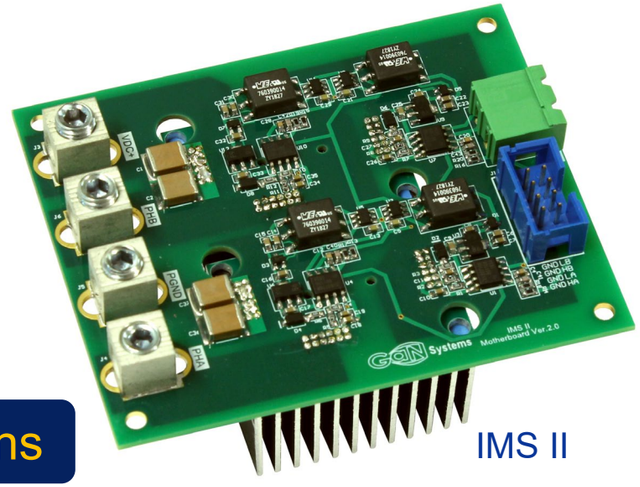
IMS I



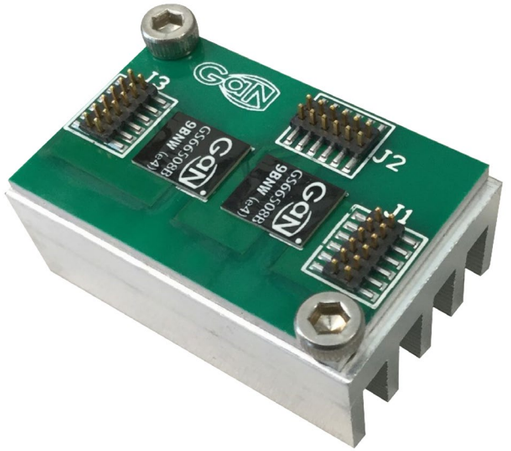
Half Bridge (650V/240A, 6mΩ)

IMS II

- Compact. Designed for mid-high power application (1~3kW).
- Applied GaN HEMT: single GS66508B or GS66516B



IMS II

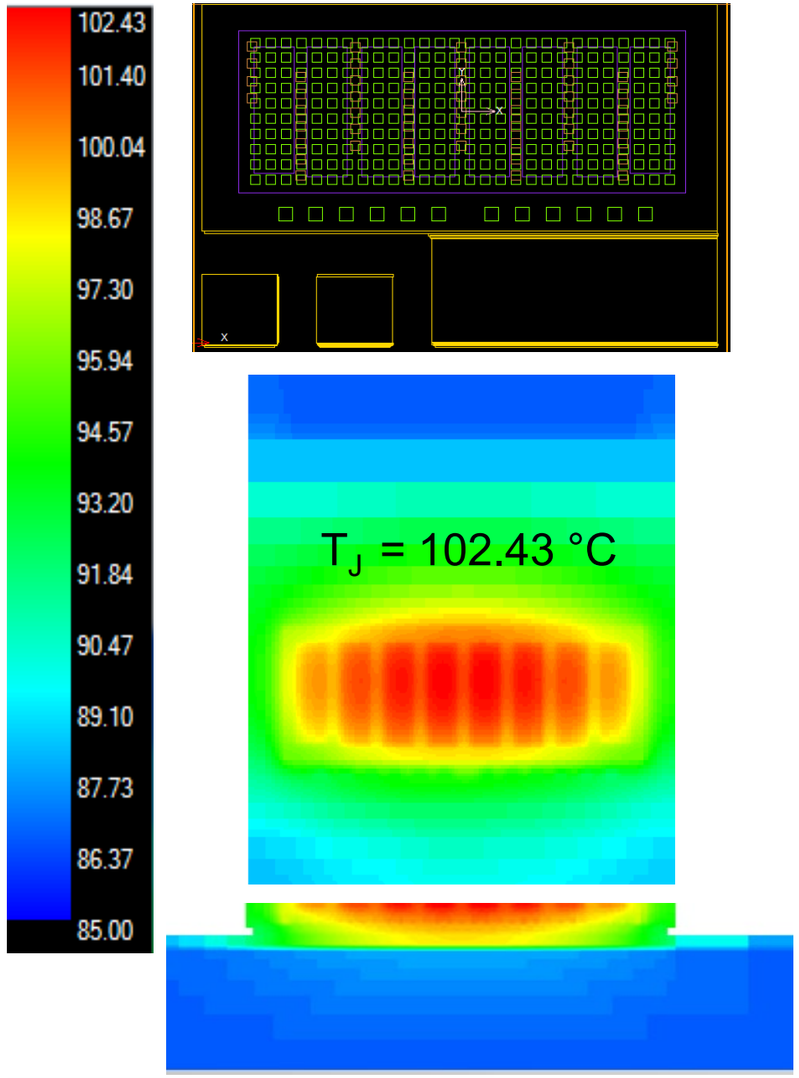


Half Bridge (650V/30A, 50mΩ)

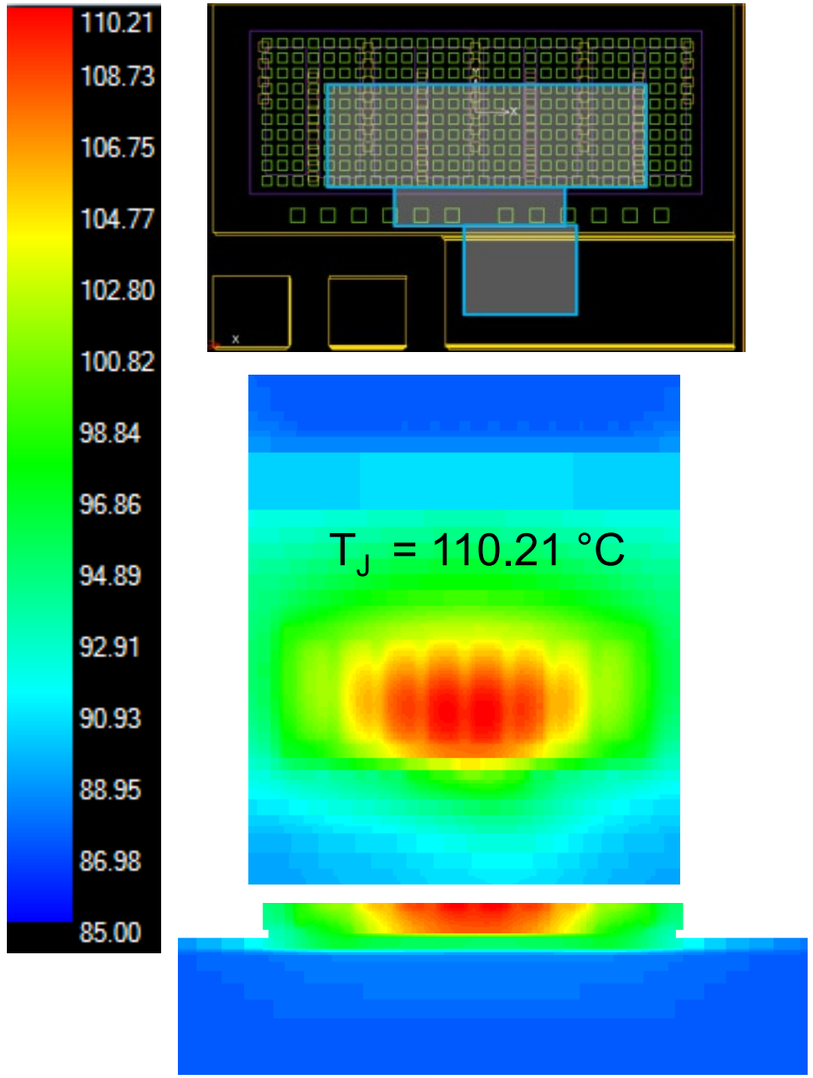
4.2. IMS Bottom-cool design – Solder voids consideration

Operating conditions: P = 7.98 W, T_{IMS} = 85 °C, GS66508B is applied

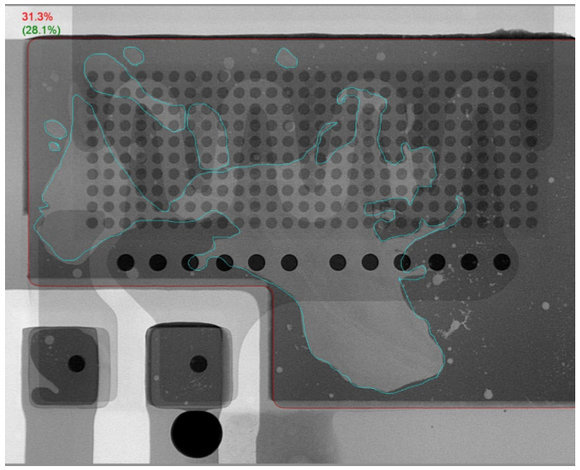
No voids under the package: $R_{\theta JIMS}$= 2.18 °C/W



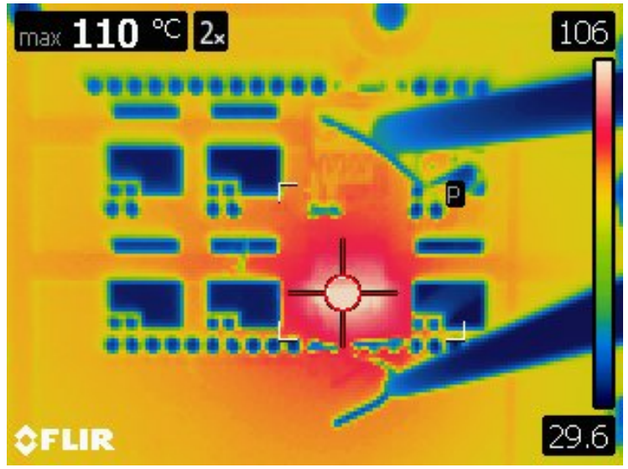
32 % voids under the package: $R_{\theta JIMS}$ = 3.16 °C/W



Measurement and Xray results



Xray results on a device with voids

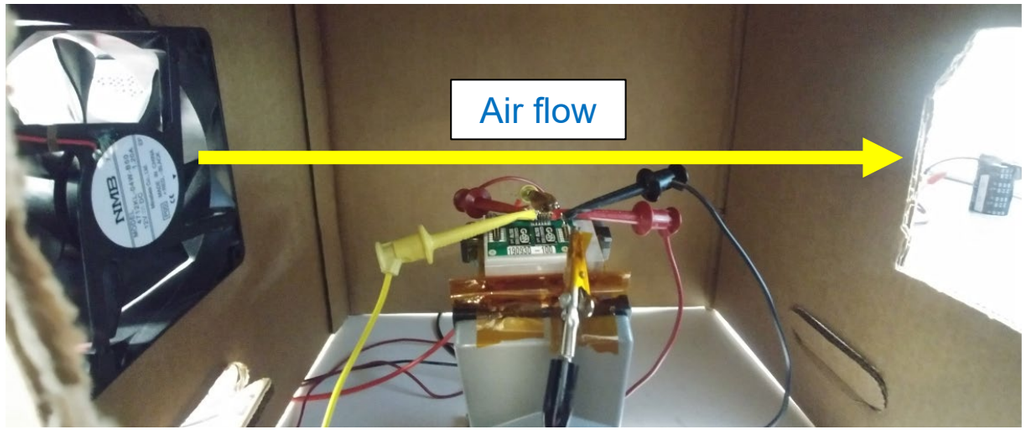


Experimental results with the device with voids

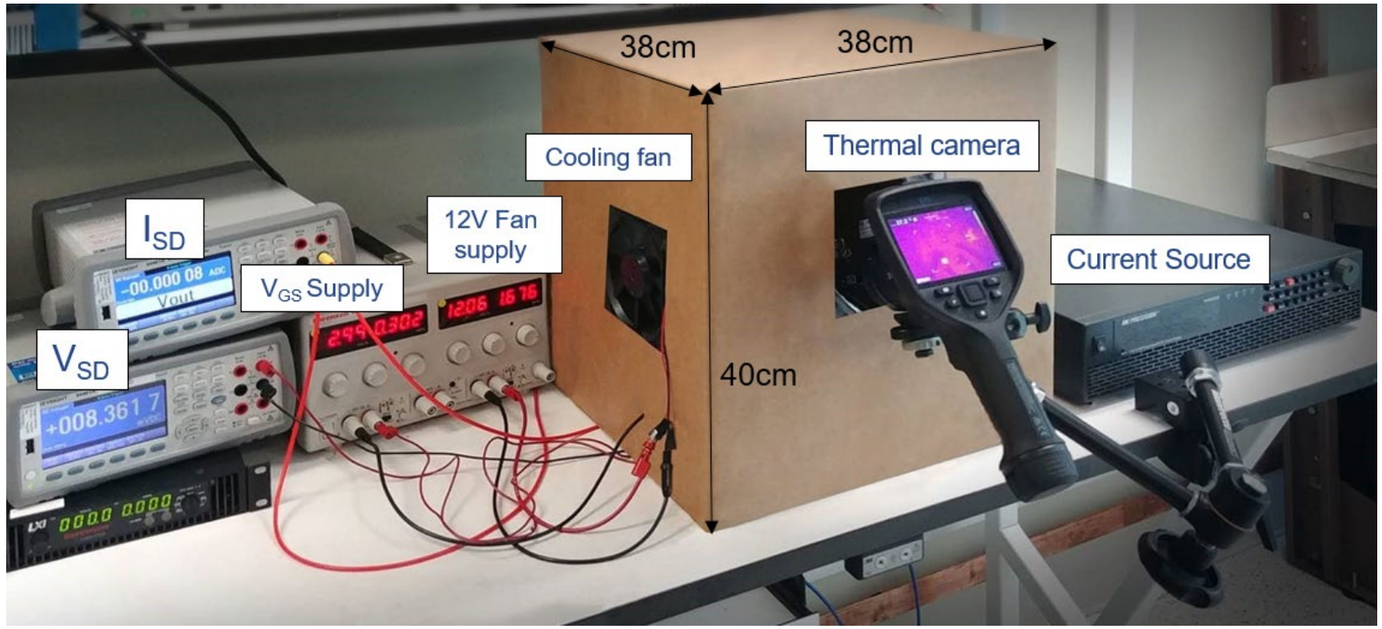
Limit voids to achieve the best IMS thermal performance

4.2. IMS Bottom-cool design – Thermal resistance measurement

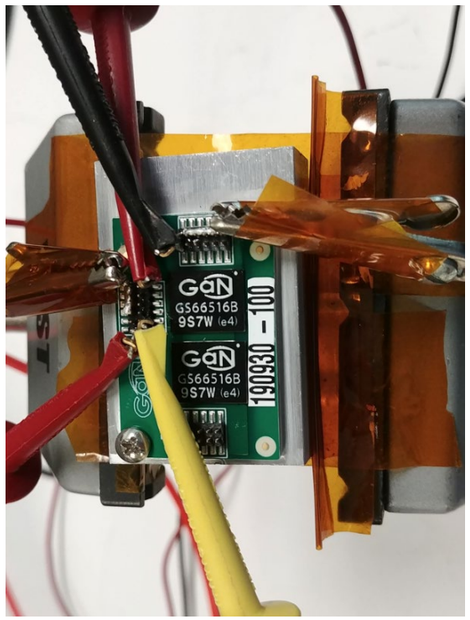
1. The $R_{\theta JA}$ for GS66516B based IMS is 2.9 °C/W.
2. GS66516B can dissipate 43 W loss per device.



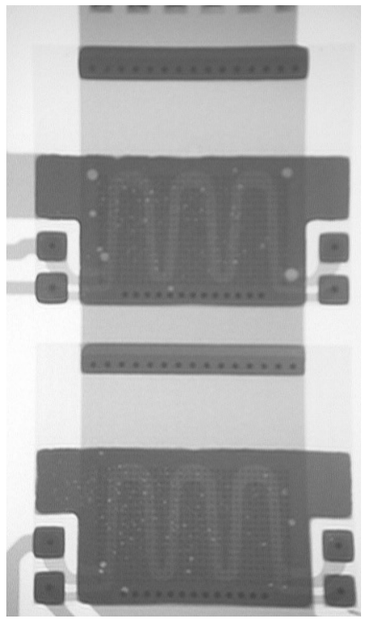
Inside setup box region



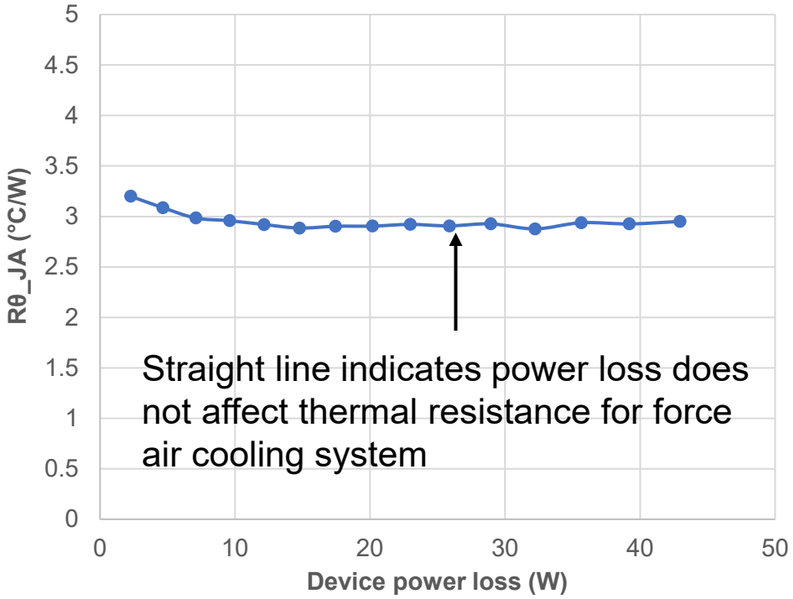
IMS force-air cooling thermal resistance test setup

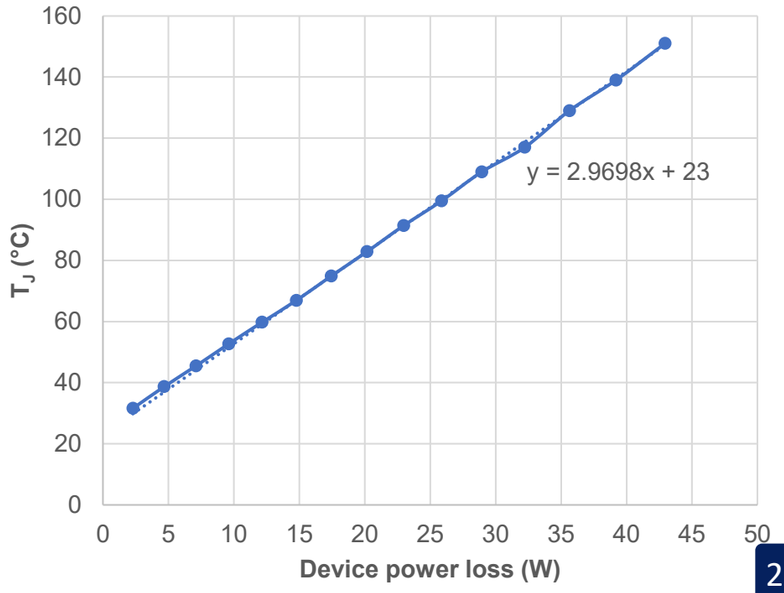


Tested GS66516B-based IMS



Minimal solder voids





Application note outline

1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. **Device selection based upon thermal consideration**
6. Loss and thermal modeling

5. Device selection from thermal consideration – single device

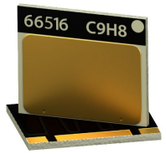
*$R_{\theta HSA}$ =1.25 °C/W
3.4x3.4x2.5 cm³

**$R_{\theta HSA}$ =1.5 °C/W
4.6x3.0x1.4 cm³

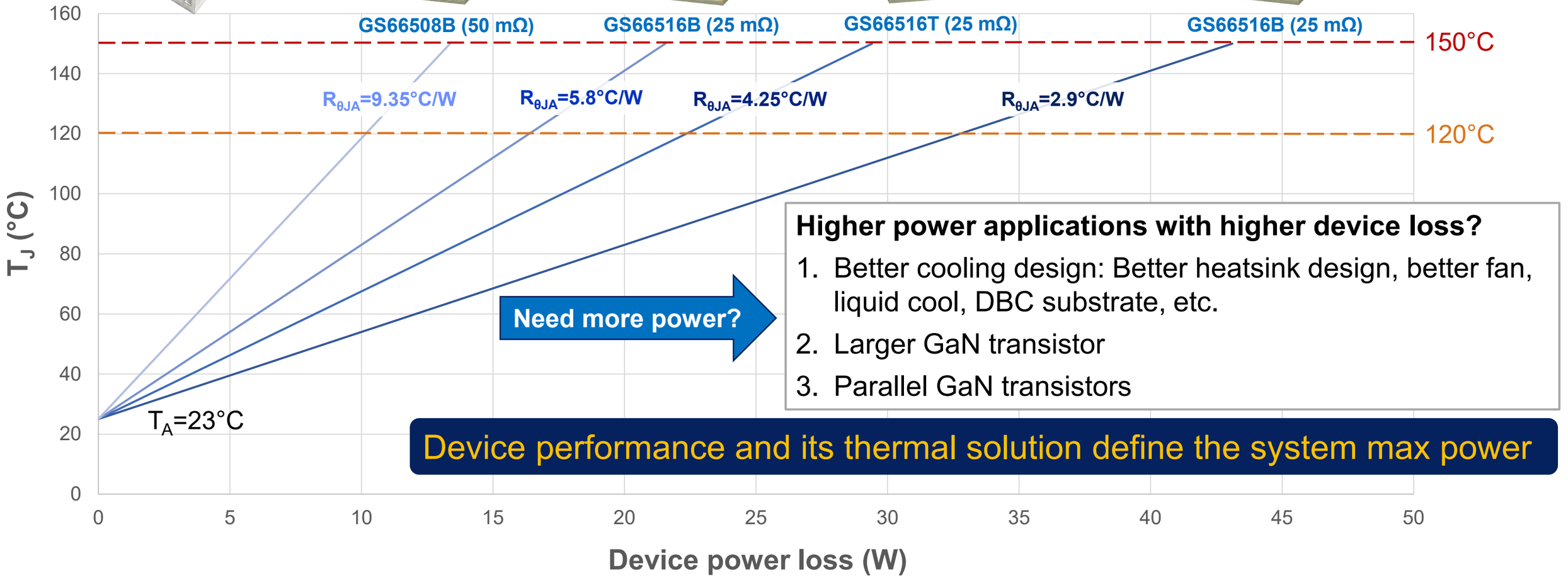
FR4 PCB
($R_{\theta HSA}$=1.25°C/W*)

FR4 PCB
($R_{\theta HSA}$ =1.25°C/W*)

Top-cool
($R_{\theta HSA}$ =1.25°C/W*)



IMS
($R_{\theta HSA}$ =1.5°C/W)**



Need more power?

Higher power applications with higher device loss?

1. Better cooling design: Better heatsink design, better fan, liquid cool, DBC substrate, etc.
2. Larger GaN transistor
3. Parallel GaN transistors

Device performance and its thermal solution define the system max power

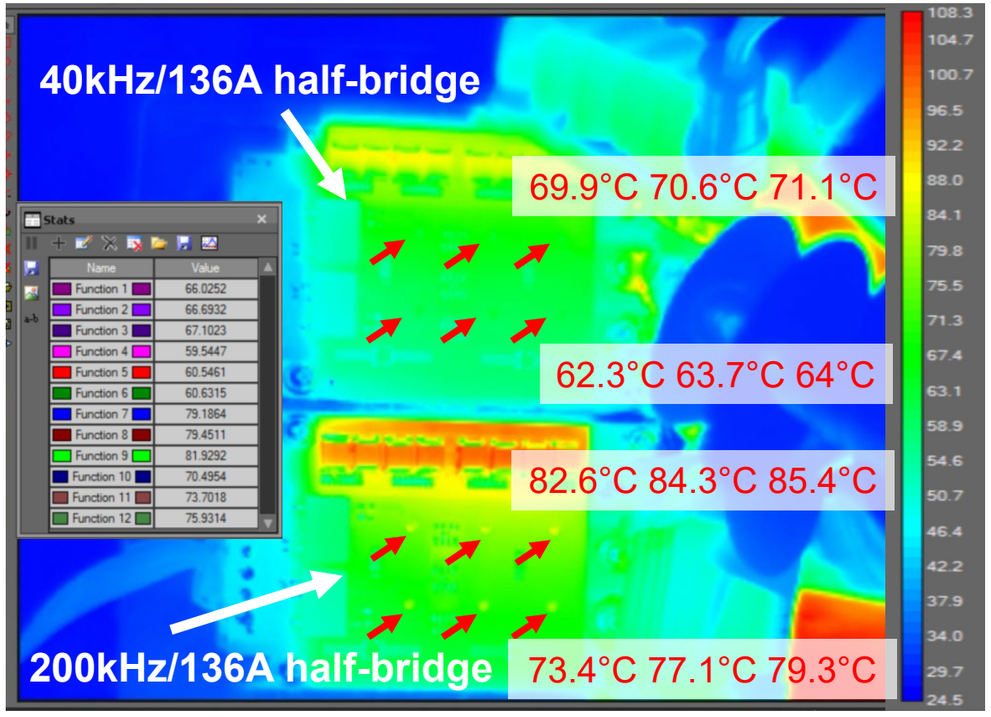
Measured device power loss vs T_J with different cooling methods – single discrete device solution

5.2 Enhance thermal performance by paralleling

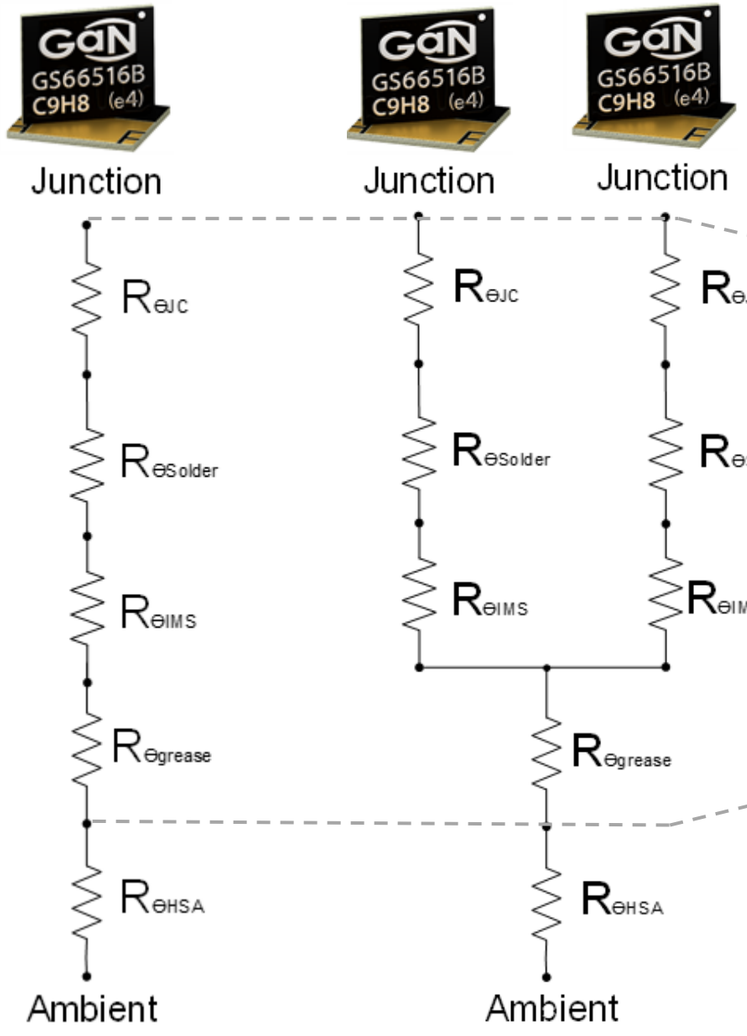
Paralleling GaN is a proven technique to increase system power

Example:

- 4xGS66516B parallel to share 136 A load current with hard-switching on/off.
- Randomly selected transistors.
- T_J difference is <6 °C for the worst case.

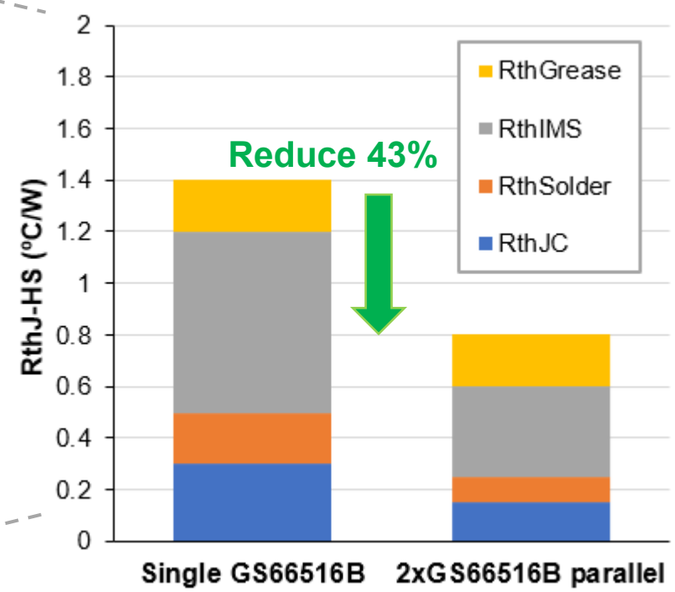


Paralleling reduces both system $R_{DS(on)}$ (electrical) and R_θ (thermal)



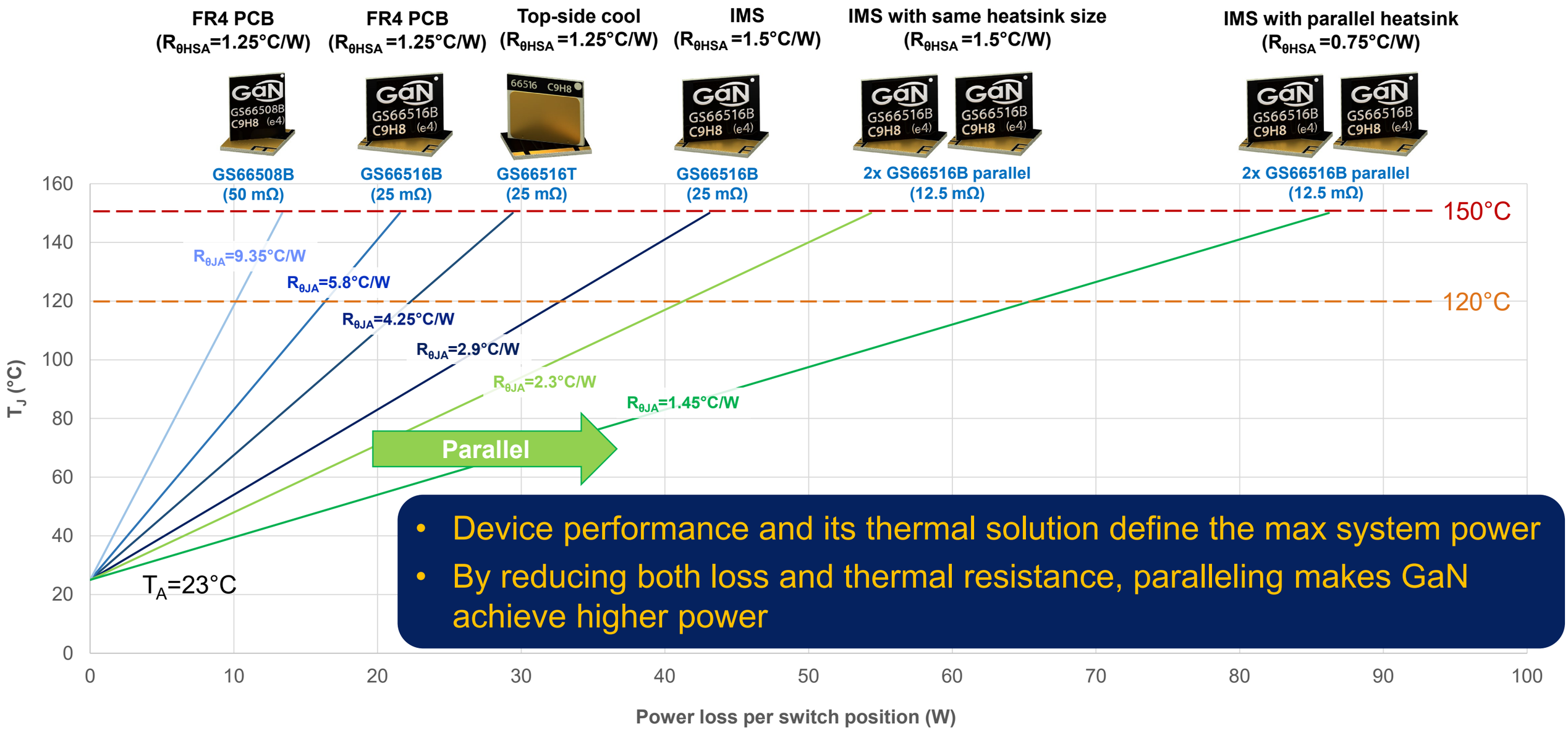
Single GS66516B thermal network

2xGS66516B parallel thermal network



Junction-to-heatsink thermal network comparison

5. Device selection from thermal consideration - including parallel



- Device performance and its thermal solution define the max system power
- By reducing both loss and thermal resistance, paralleling makes GaN achieve higher power

Device loss vs T_J with different cooling methods including parallel solution

Application note outline

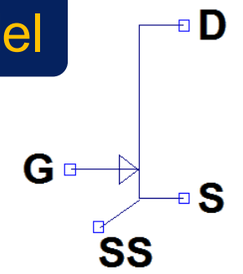
1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. **Loss and thermal modeling**
    - 6.1 SPICE modeling
    - 6.2 PLECS modeling

6.1. SPICE modeling

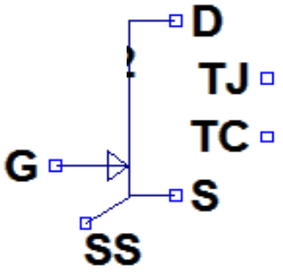
GaN Systems provides a two-level SPICE model. For thermal modeling, use L3 model

Definitions of model levels

Suffix	Level	Terminals	Description
_L1	1	G, D, S, SS (if applicable)	General electrical simulations on application/converter level circuits. Focus on simulation speed.
_L3	3	G, D, S, SS (if applicable), Tc, Tj	In addition to L1, L3 also includes the thermal model and package stray inductance.



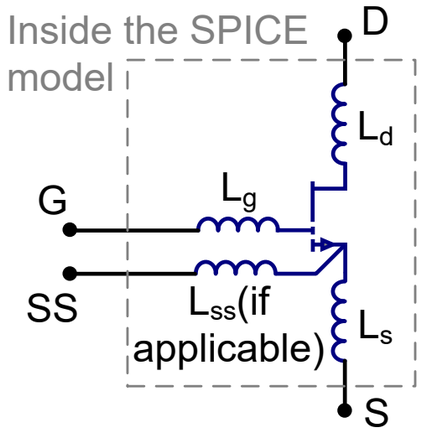
L1 device symbol



L3 device symbol

Functions of model levels

Functions	Level 1	Level 3
IV performance as a function of temperature	✓	✓
Voltage-dependent capacitance	✓	✓
Thermal model	×	✓
Package stray inductance	×	✓

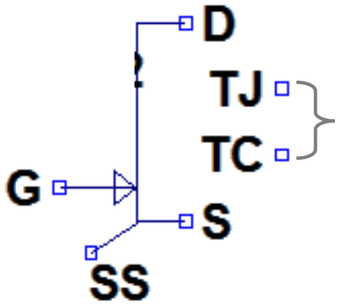


Modeled parasitic inductance in L3

6.1. SPICE modeling

Junction-to-case thermal modeling

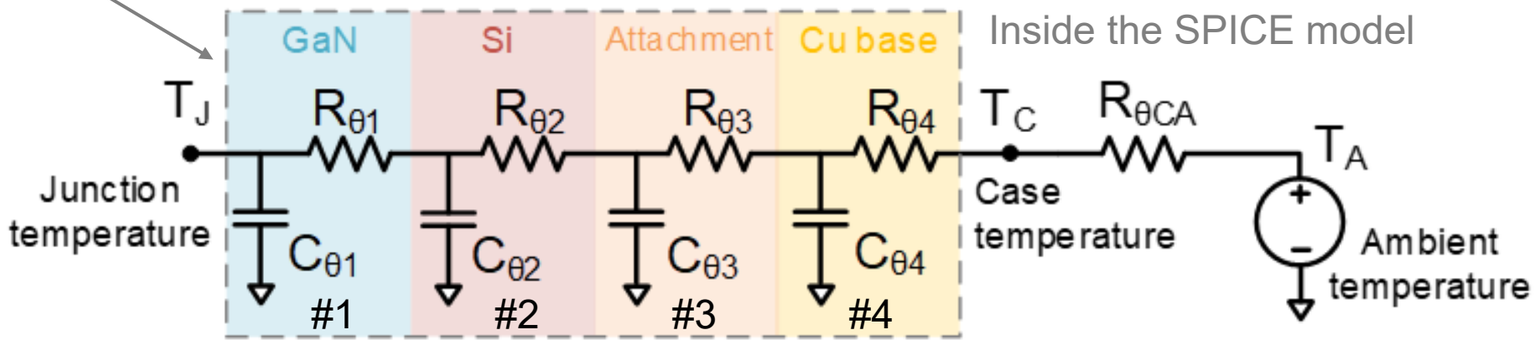
4-stage Cauer RC thermal model to accurately represent device



L3 device symbol

Cauer model is applied for junction-to-case thermal modeling due to:

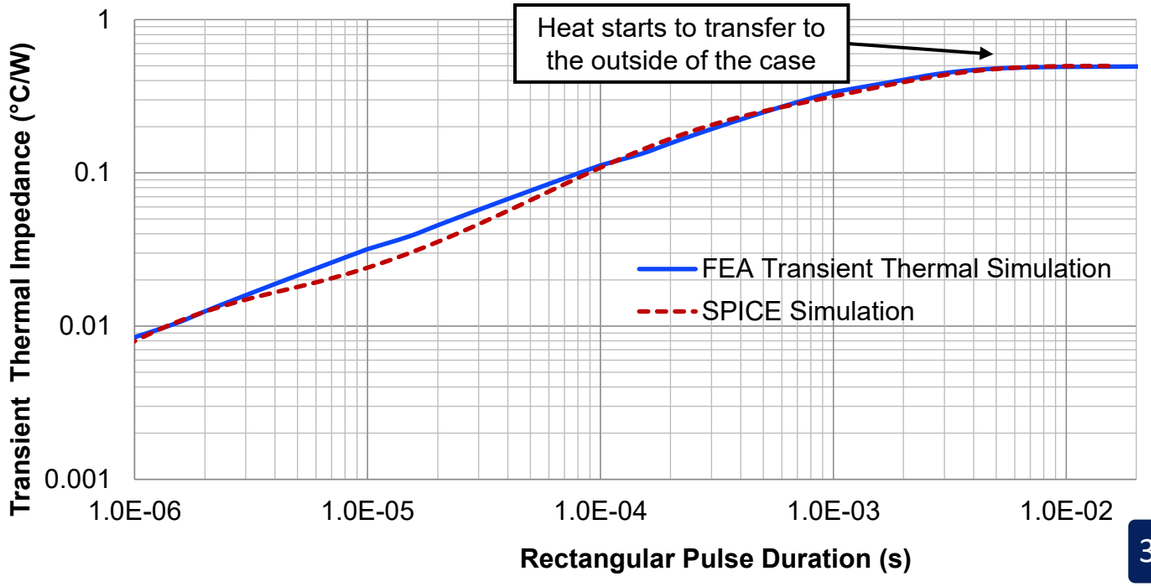
1. Unlike the Foster model (curve-fitting model), Cauer RC network is based on the physical property and packaging structure
2. The RC elements are assigned to the package layers



Example: GS66508B $R_{\theta JC}$ modeling

	R_θ (°C/W)	C_θ (W·s/°C)
#1	0.015	8.0E-05
#2	0.23	7.4E-04
#3	0.24	6.5E-03
#4	0.015	2.0E-03

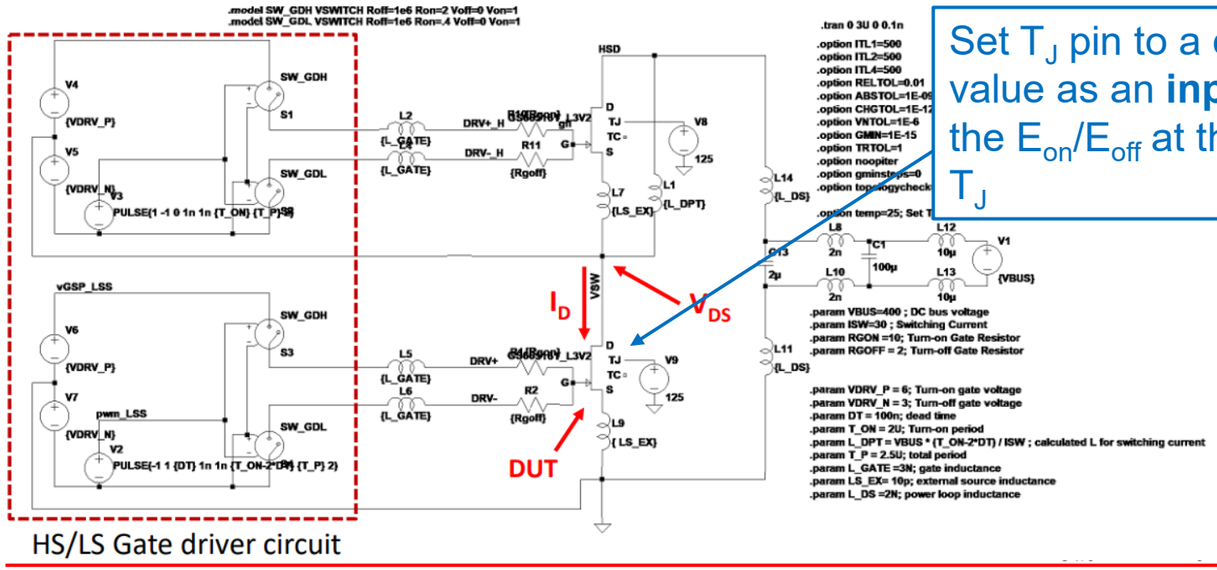
GS66508B Cauer RC model parameters



6.1. SPICE modeling

T_J pin can be used as an input or output, depends on the simulation purpose

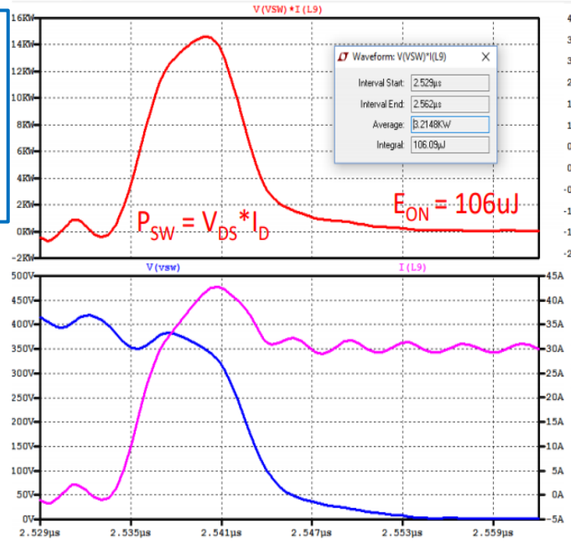
GAN SYSTEMS SWITCHING LOSS DOUBLE PULSE TEST BENCH



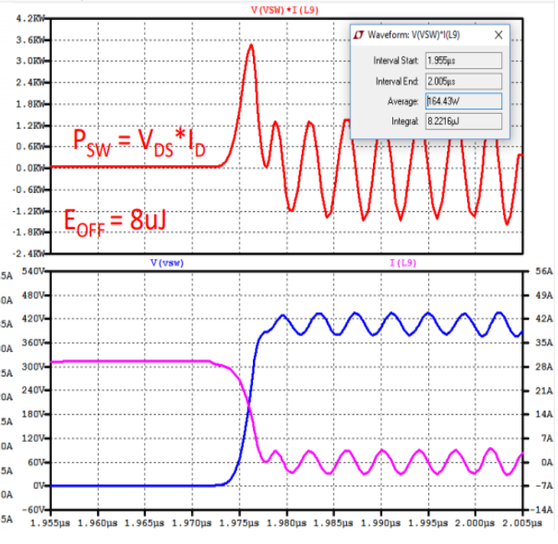
HS/LS Gate driver circuit

Set T_J pin to a constant value as an **input** to check the E_{on}/E_{off} at the desired T_J

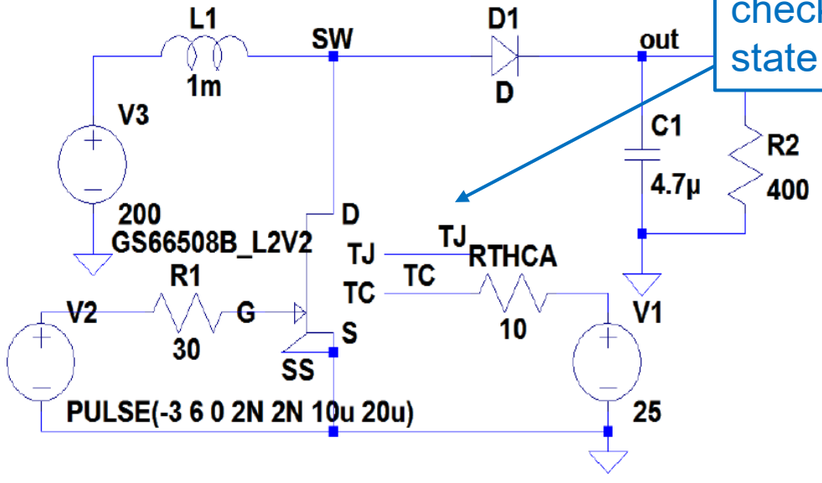
400V/30A Turn-on



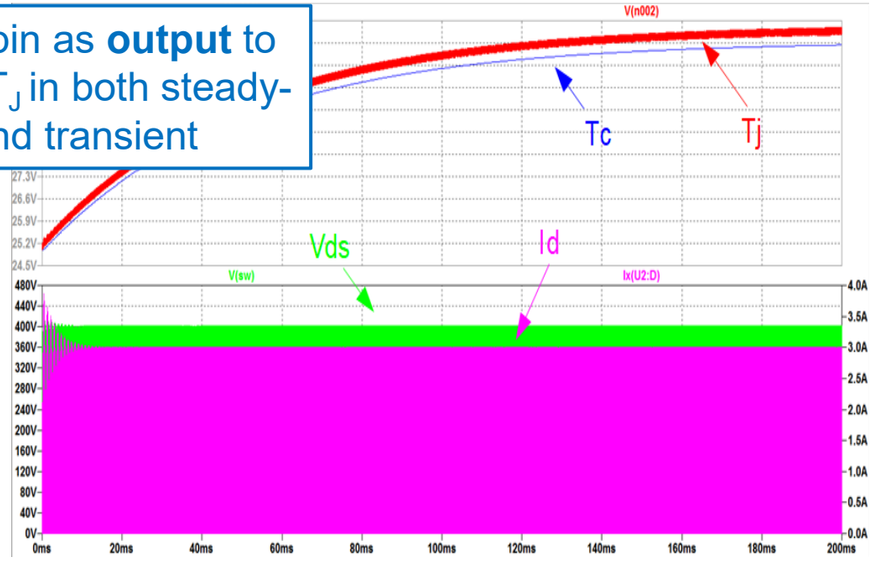
400V/30A Turn-off

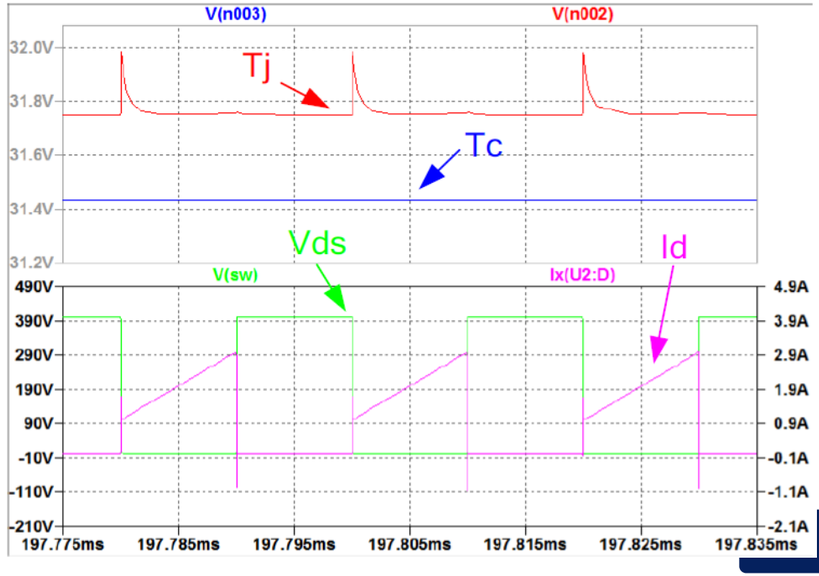


Continuous Converter Simulation



Set T_J pin as **output** to check T_J in both steady-state and transient

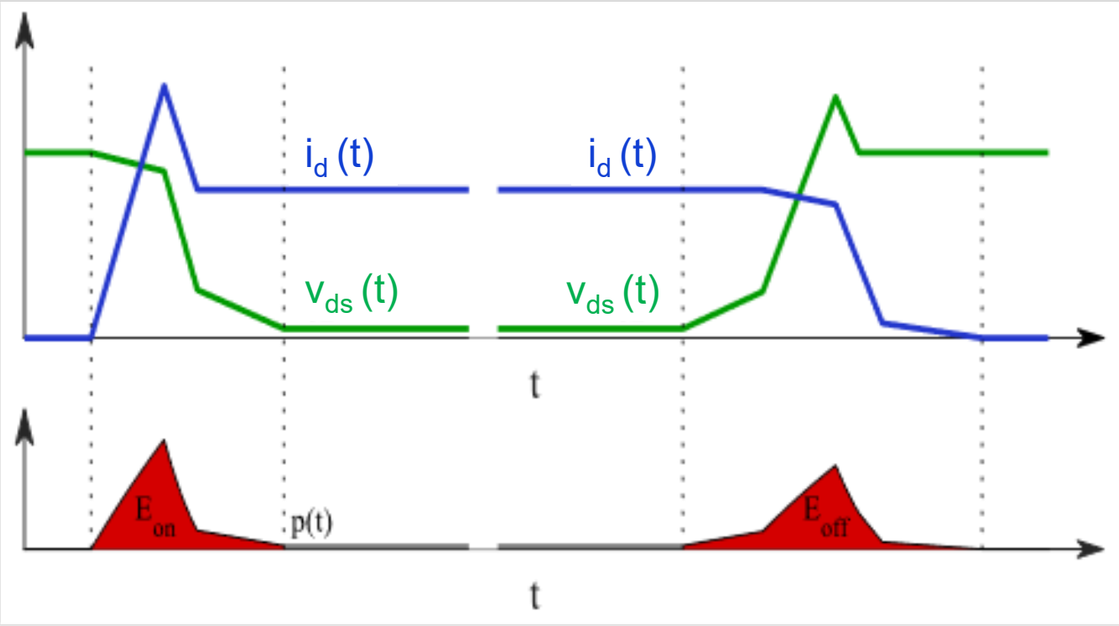




6.2. PLECS modeling

Device-level simulation
(LTspice and Pspice)

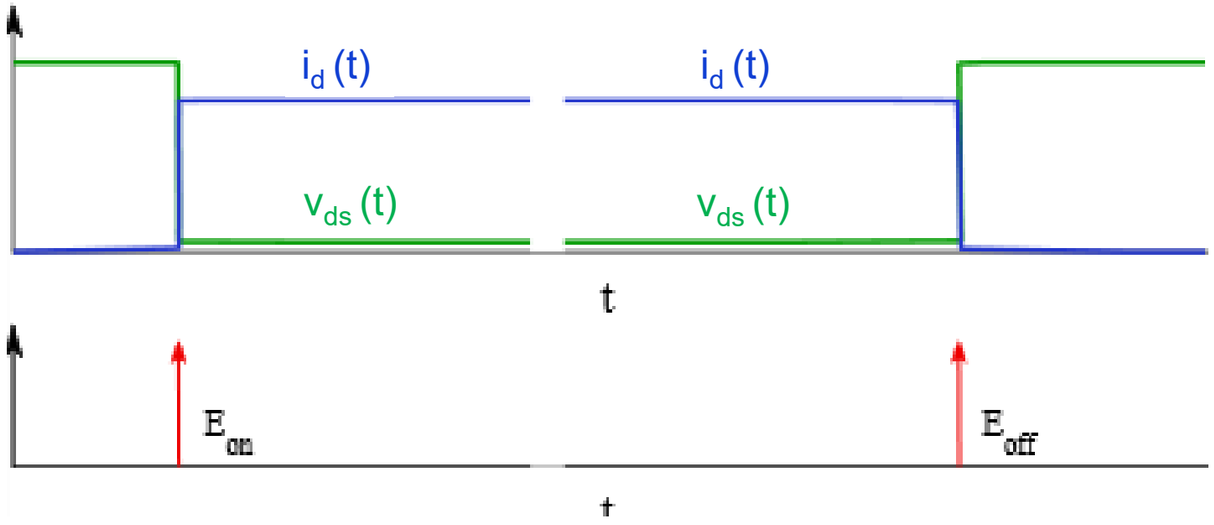
- Device characteristics (Q_g, C_{oss}/C_{iss}, IV/CV curve, E_{on}/E_{off})
- Simple system simulation (double-pulse test, buck, boost, etc.)
- See parasitic effect on switching performance



Transient hard-switching on and its loss in SPICE

Converter/system-level simulation
(PLECS)

- Simplify the switching transient
- Observe converter operating waveforms
- Can handle complicated device-based system-level simulation/analysis

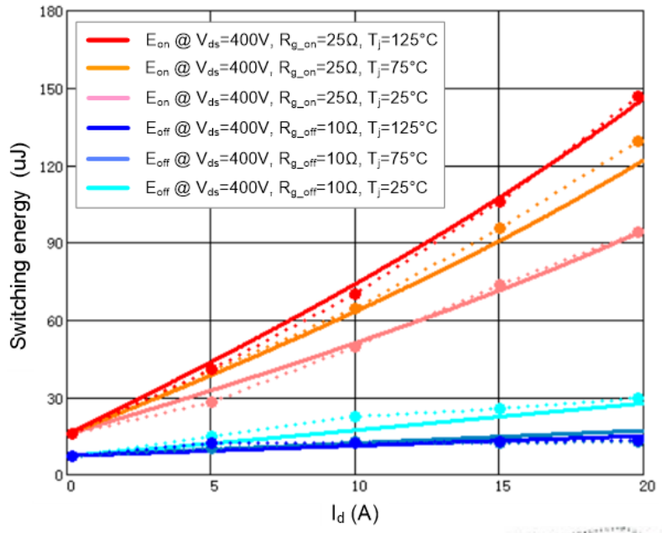


Hard-switching on and its loss in PLECS

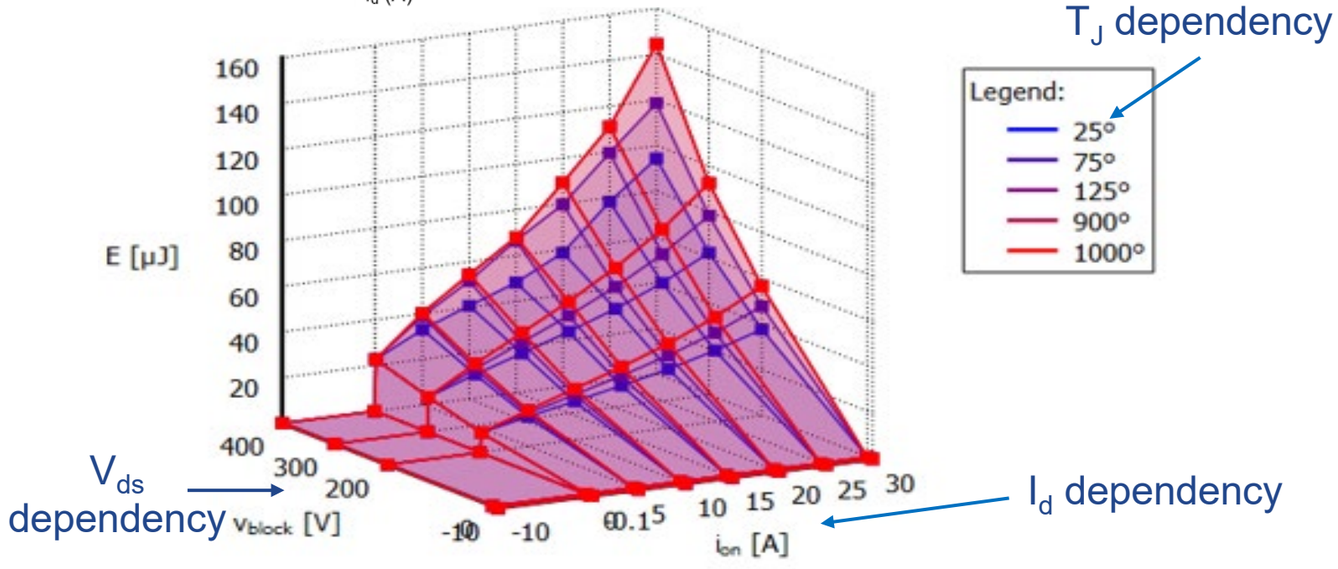
LTSPICE, PSPICE, and PLECS models assist system design to maximize performance

6.2. PLECS modeling

Switching loss modeling



- An E_{on}/E_{off} scaling method is developed by GaN Systems.
- E_{on}/E_{off} data can be scaled to different T_J, V_{ds}, and R_g.

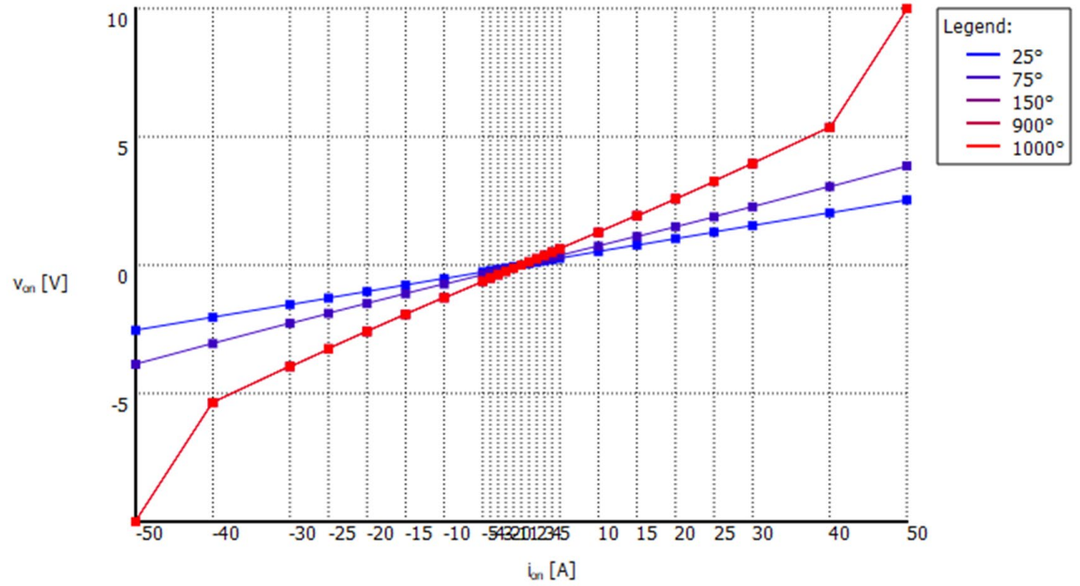


E_{on} in PLECS modeling

R_g-dependent equation:

$$E_{on}(v,i,T,E,Rgon,Rgoff,vgsoff,g) = ((Rgon-10)*(v*i)/2*(1.68e-9+2.2e-9*(i/24.4)/(1.3+i/24.4))/(6-1.3-i/24.4)+E)*g$$

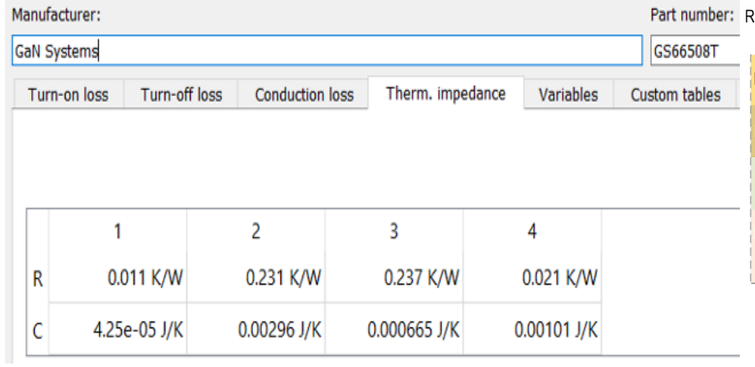
Conduction loss modeling

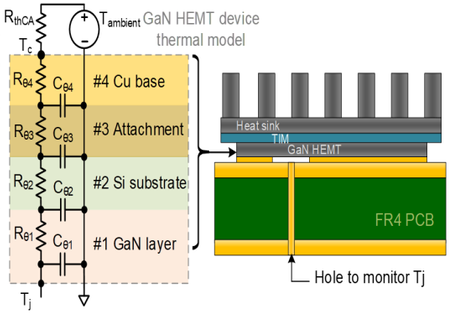


Deadtime loss modeling:

$$v_{on}(i,T,v,Rgon,Rgoff,vgsoff,g) = v-(i<0)*(1-g)*(1.3-vgsoff)$$

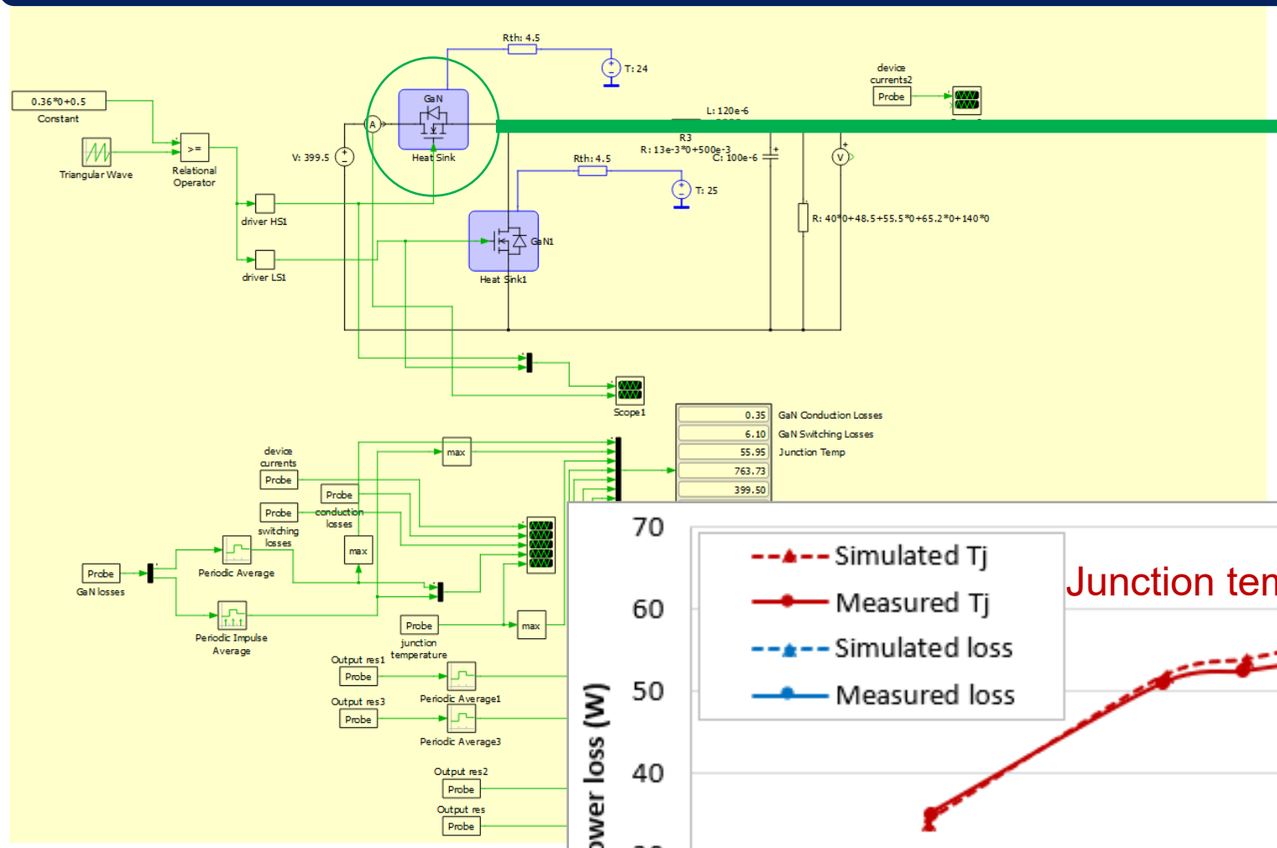
Thermal modeling (junction-to-case)

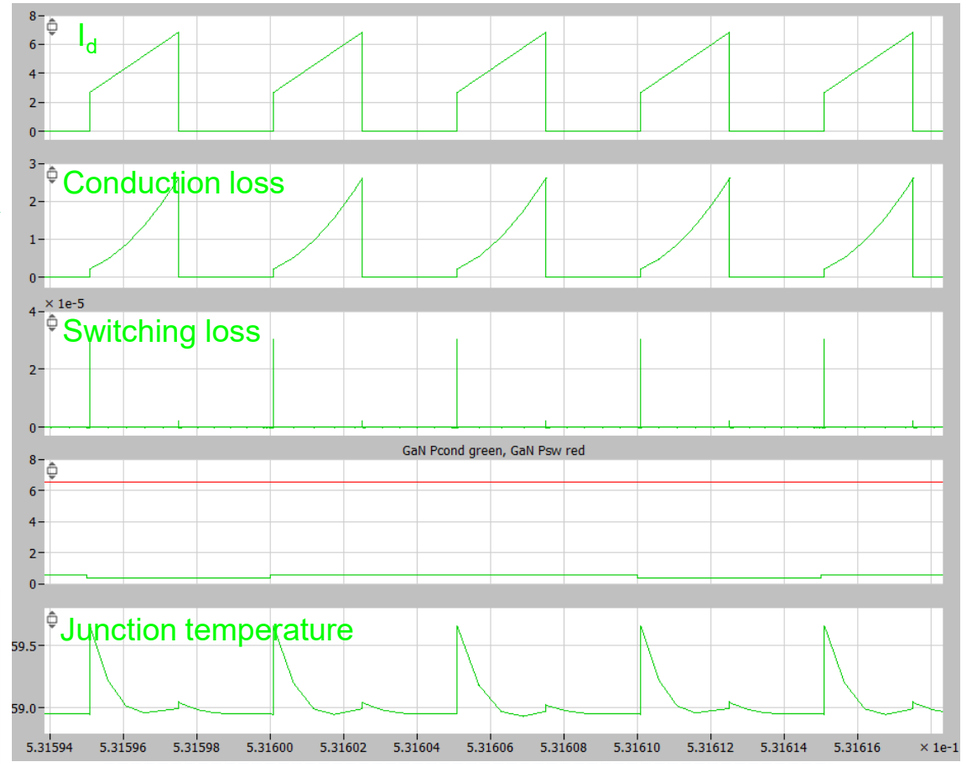


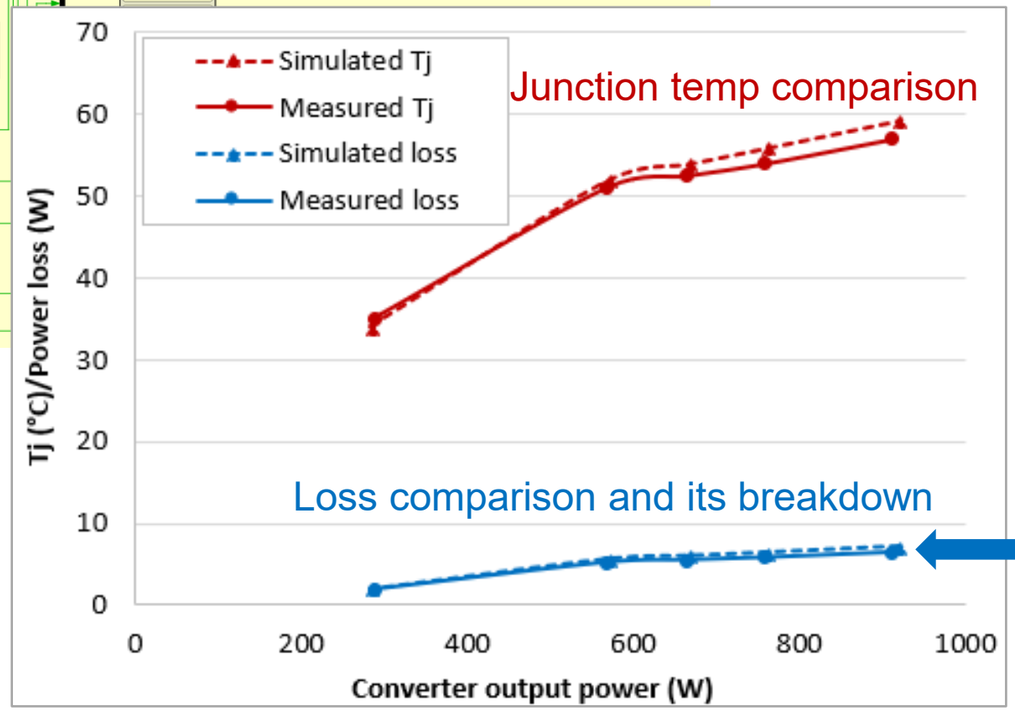


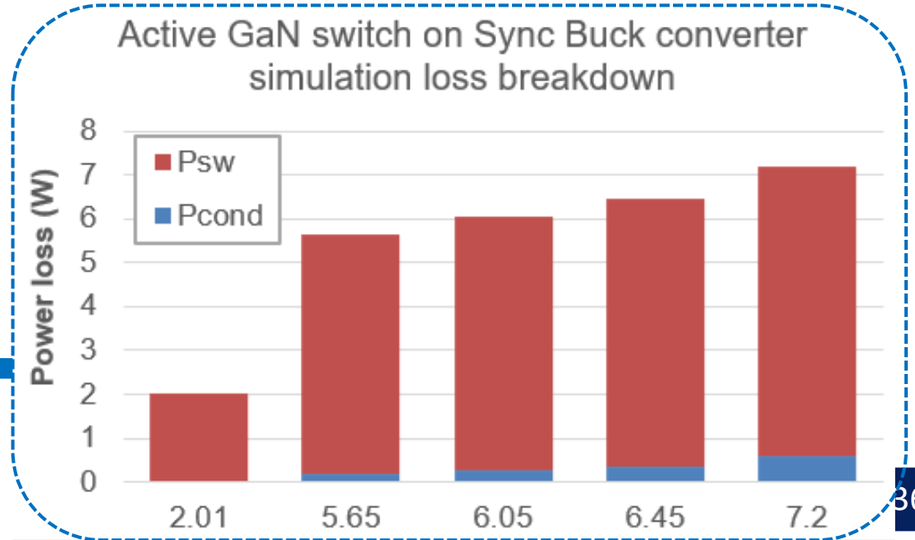
6.2. PLECS modeling verification

PLECS device model verified by a Buck converter example









Based on GS66508

F_{sw}=200 kHz,

V_{in}=400 V,

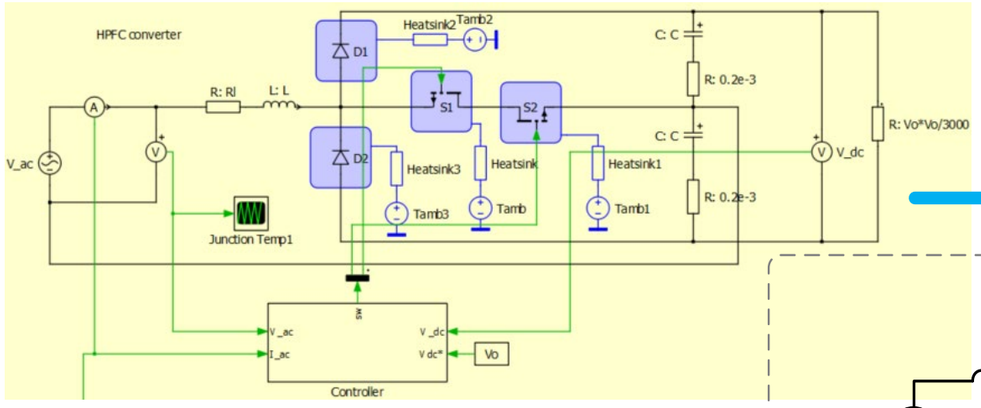
V_o=193 V

$R_{\theta CA}$=4.5 °C/W

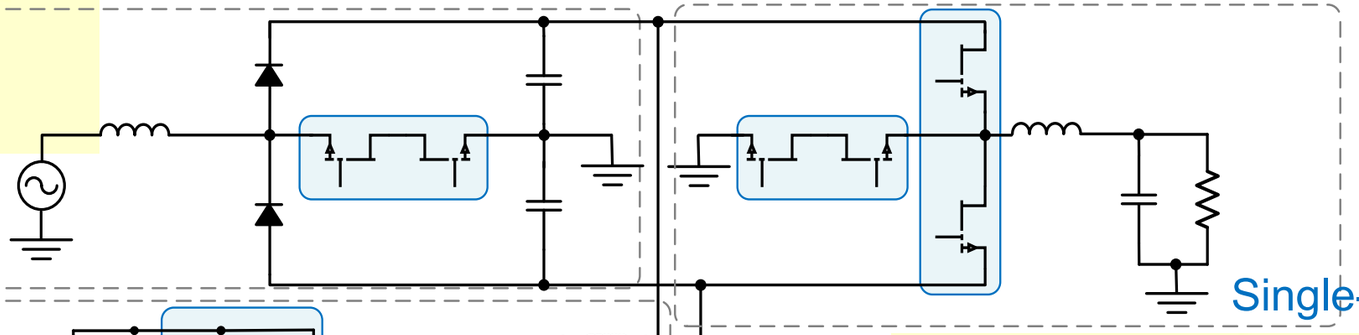
6.2. PLECS modeling – System loss and thermal analysis

Example: UPS system

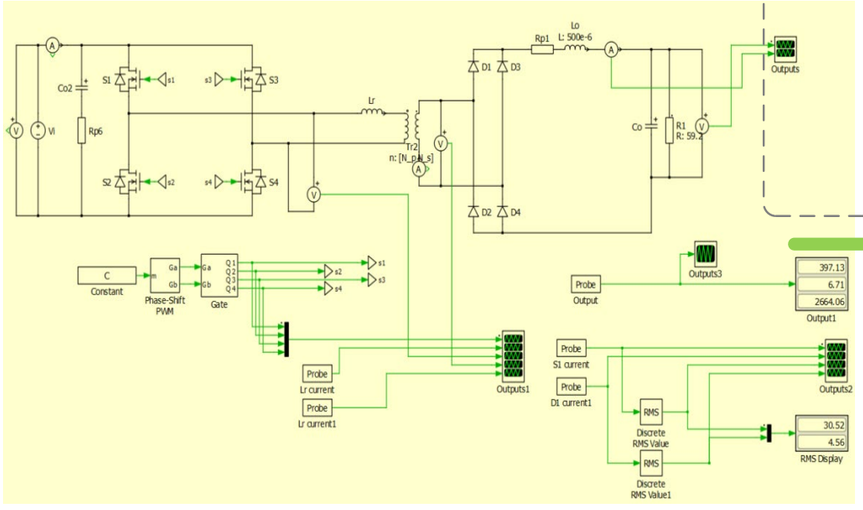
PLECS model can be used for system-level analysis



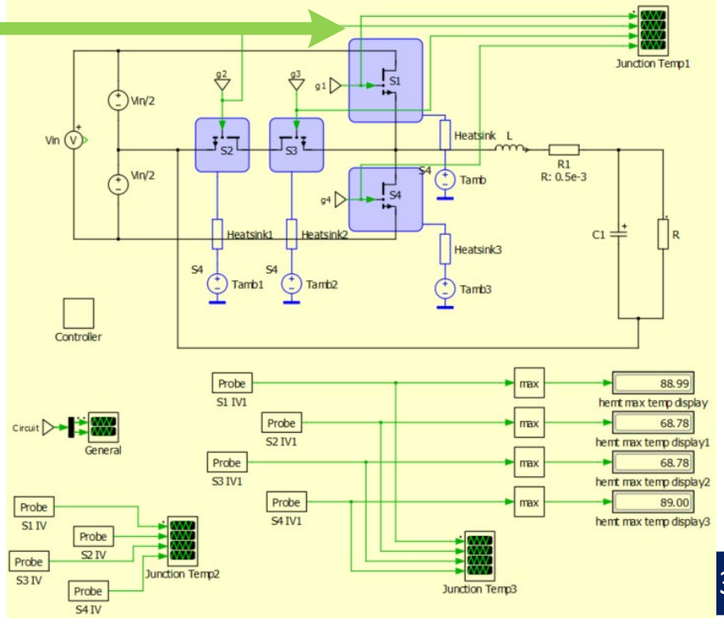
Bridgeless PFC



Single-phase inverter



Isolated DC/DC



6.2. PLECS modeling – Online simulation tool

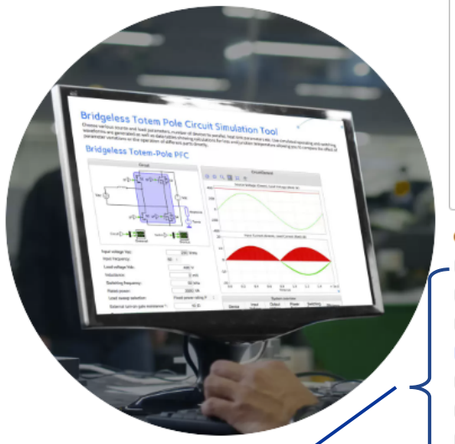
GaN Systems also provide online simulation tool based on PLECS model

Welcome to the GaN Systems Circuit Simulation Tools

The Circuit Simulation Tool allows you to compare application conditions by implementing specific operating values. Choose various source and load parameters, number of devices to parallel, heat sink parameters etc. Live simulated operating and switching waveforms are generated as well as data tables showing calculations for loss and junction temperature allowing you to compare the effect of parameter variations or the operation of different parts directly.

You may also download the PLECS device model files for GaN Systems' transistors.

- BRIDGELESS TOTEM-POLE PFC
- SINGLE-PHASE, 2-LEVEL INVERTER
- SINGLE-PHASE, 3-LEVEL HALF-BRIDGE INVERTER
- SINGLE-PHASE T-TYPE 3-LEVEL INVERTER
- ISOLATED HALF-BRIDGE LLC CONVERTER
- ISOLATED PHASE-SHIFT FULL BRIDGE CONVERTER
- THREE-PHASE TRACTION INVERTER
- DUAL ACTIVE BRIDGE

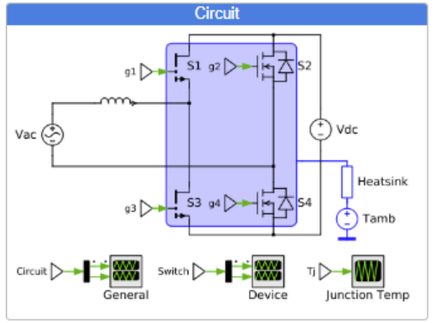


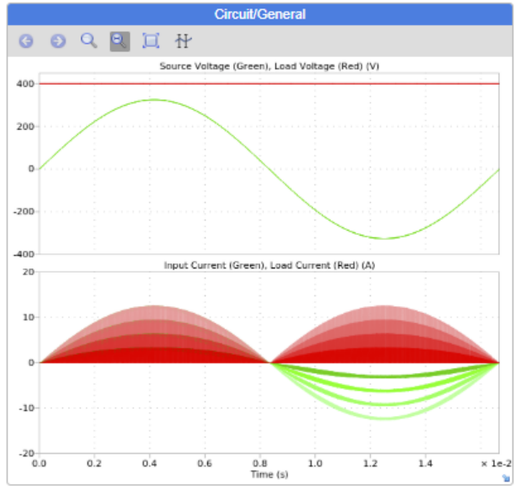
GaN PLECS model for both 100V and 650V device

All GaN Systems' device models and 8 topologies are available online
https://gansystems.com/design-center/circuit-simulation-tools/

Bridgeless Totem Pole Circuit Simulation Tool

Choose various source and load parameters, number of devices to parallel, heat sink parameters etc. Live simulated operating and switching waveforms are generated as well as data tables showing calculations for loss and junction temperature allowing you to compare the effect of parameter variations or the operation of different parts directly. You may also download the PLECS device model files for GaN Systems' transistors.





GaN HEMT:

- ☐ GS66502B 650 V, 7.5 A, 200 mΩ
- ☐ GS66504B 650 V, 15 A, 100 mΩ
- ☐ GS66506T 650 V, 22.5 A, 67 mΩ
- ☑ GS66508B/T/P 650 V, 30 A, 50 mΩ
- ☐ GS66516B/T 650 V, 60 A, 25 mΩ
- ☐ GS-065-008-1 650 V, 8 A, 225 mΩ
- ☐ GS-065-011-1 650 V, 11 A, 150 mΩ
- ☐ GS61004B 100 V, 45 A, 15 mΩ
- ☐ GS61008P/T 100 V, 90 A, 7 mΩ

Input voltage Vac:	230	Vrms
Input frequency:	60	
Load voltage Vdc:	400	V
Inductance:	2	mH
Switching frequency:	50	kHz
Rated power:	2000	VA
Load sweep selection:	Sweep power rating P	

Scaling factor for power rating:

- ☑ 25%
- ☑ 50%
- ☑ 75%
- ☑ 100%

External turn-on gate resistance [1]:	10	Ω
External turn-off gate resistance [2]:	2	Ω
Turn-off gate-source voltage:	-2	V
Deadtime:	100	ns
Number of paralleled GaN transistors:	1	

System overview

GaN Device	MOSFET Rdson [3]	Input Voltage	Output Voltage	Power Rating	Switching Frequency	Efficiency
GS66508B/T/P	155 mΩ	230 V	400 V	488 W	50 kHz	99.48 %
GS66508B/T/P	128 mΩ	230 V	400 V	991 W	50 kHz	99.35 %
GS66508B/T/P	105 mΩ	230 V	400 V	1.492 kW	50 kHz	99.09 %
GS66508B/T/P	86 mΩ	230 V	400 V	1.992 kW	50 kHz	98.70 %

GaN transistor thermal overview

Device	Switching	Conduction	Combined Losses [4]	Junction Temperature
GS66508B/T/P	1.35 W	0.32 W	2.53 W	32 °C
GS66508B/T/P	1.62 W	1.22 W	6.46 W	40 °C
GS66508B/T/P	1.91 W	2.89 W	13.56 W	53 °C
GS66508B/T/P	2.33 W	5.81 W	25.89 W	76 °C

Summary

Conclusions

- Good thermal design improves GaN transistor and system performance.
- Maximizing electrical **and** thermal design of GaN-based systems increases performance in soft-switching to hard-switching applications and operates efficiently from several watts to many kilowatts.

Key design tips provided in this app note

- Top-cool thermal design: TIM and heat sink mounting
- Bottom-cool thermal design: PCB design and solder voids
- Device selection including paralleling options
- Modeling tools to assist with power loss calculation and thermal design

References

For more reading…

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5. GaN Systems, LTspice Model User Guide. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/05/LTspice-Model-User-Guide.pdf
6. J. Lu, R. Hou and D. Chen, "Loss Distribution among Paralleled GaN HEMTs," in Proc. *2018 IEEE ECCE*, Portland, OR, 2018.
7. R. Hou, J. Lu, and D. Chen, “Parasitic capacitance E_{qoss} loss mechanism, calculation, and measurement in hard-switching for GaN HEMTs,” in *Proc. 2018 IEEE APEC*, San Antonio, TX, 2018.
8. J. L. Lu, R. Hou and D. Chen, "Opportunities and design considerations of GaN HEMTs in ZVS applications," in Proc. *2018 IEEE APEC*, San Antonio, TX, 2018.
9. R. Hou, J. Xu, and D. Chen, “Multivariable turn-on/turn-off switching loss scaling approach for high-voltage GaN HEMTs in a hard-switching half-bridge configuration,” in *Proc. 2017 IEEE WiPDA*, Albuquerque, NM, 2017.
10. R. Hou, Y. Shen, H. Zhao, H. Hu, J. Lu and T. Long, "Power Loss Characterization and Modeling for GaN-Based Hard-Switching Half-Bridges Considering Dynamic On-State Resistance," in *IEEE Transactions on Transportation Electrification,* Jun. 2020.

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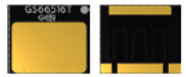
GS66502B
7.5 A, 200 mΩ
6.6 x 5.0 mm

GS66504B
15 A, 100 mΩ
6.6 x 5.0 mm

GS66506T
22 A, 67 mΩ
5.6 x 4.5 mm

GS66508T
30 A, 50 mΩ
7.0 x 4.5 mm

GS66508B
30 A, 50 mΩ
8.4 x 7.0 mm

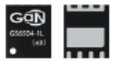


GS66516T
60 A, 25 mΩ
9.0 x 7.6 mm

GS66516B
60 A, 25 mΩ
11.0 x 9.0 mm

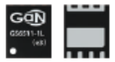
GS-065-080-1-D1
80 A, 18 mΩ
6.6 x 5.6 mm

GS-065-150-1-D1
150 A, 10 mΩ
12.7 x 5.6 mm



GS-065-004-1-L
4 A, 450 mΩ
5.0 x 6.0 mm

GS-065-008-1-L
8 A, 225 mΩ
5.0 x 6.0 mm



GS-065-011-1-L
11 A, 150 mΩ
5.0 x 6.0 mm

100 V GaN

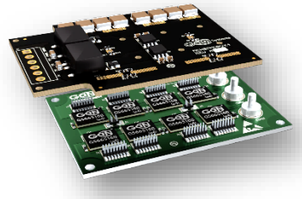
GS61004B
45 A, 15 mΩ
4.6 x 4.4 mm

GS61008P
90 A, 7 mΩ
7.6 x 4.6 mm

GS61008T
90 A, 7 mΩ
7.0 x 4.0 mm

Many Eval Kits & Reference Designs

Half bridge power stage



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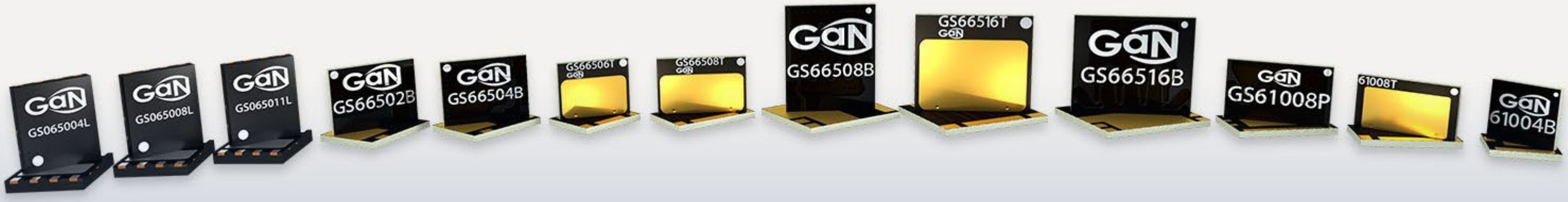
GS065004L
GS065008L
GS065011L
GS66502B
GS66504B
GS66506T
GS66508T
GS66508B
GS66516T
GS66516B
GS61008P
61008T
61004B

GaN Systems