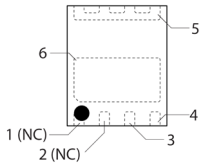
GS-065-004-1-L
Bottom-side cooled 650 V E-mode GaN transistor
Preliminary Datasheet

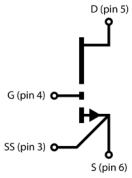
Features

- 650 V enhancement mode power switch
- Bottom-side cooled
- $R_{DS(on)}$ = 500 mΩ
- $I_{DS(max)}$ = 3.5 A
- Small 5x6 mm PDFN package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Source Sense pad for optimized gate drive
- Reverse current capability
- Zero reverse recovery loss
- RoHS 6 compliant

Package Outline



Circuit Symbol



Applications

- Power Adapters
- LED lighting drivers
- Fast Battery Charging
- LLC Converters
- Power Factor Correction
- Appliance Motor Drives
- Wireless Power Transfer
- Industrial power supplies

Description

The GS-065-004-1-L is an enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. The GS-065-004-1-L is a bottom-side cooled transistor that offers low junction-to-case thermal resistance. These features combine to provide very high efficiency power switching.

Submit datasheet feedback

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-40 to +150	°C
Storage Temperature Range	T_S	-40 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C)	I_{DS}	3.5	A
Continuous Drain Current (T_{case} = 100 °C)	I_{DS}	2.5	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	7.1	A

(1) Pulse $\leq$ 1 µs

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	4.0	°C /W
Thermal Resistance (junction-to-ambient) (note 2)	$R_{\Theta JA}$	40	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(2) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS-065-004-1-L-MR	5x6 mm PDFN	Mini-Reel	250	7″	12mm
GS-065-004-1-L -TR	5x6 mm PDFN	Tape-and-Reel	TBD	13″	12mm

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	V_{GS} = 0 V I_{DSS} = 12.5 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		500		mΩ	V_{GS} = 6 V, T_J = 25°C I_{DS} = 1 A
Drain-to-Source On Resistance	$R_{DS(on)}$		1194		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 1 A
Gate-to-Source Threshold	$V_{GS(th)}$		1.4		V	V_{DS} = V_{GS}, I_{DS} = 0.8 mA
Gate-to-Source Current	I_{GS}		18		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		4		V	V_{DS} = 400 V, I_{DS} = 4 A
Drain-to-Source Leakage Current	I_{DSS}		0.2		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		45		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		0.65		Ω	
Input Capacitance	C_{ISS}		30		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		7.7		pF	
Reverse Transfer Capacitance	C_{RSS}		0.2		pF	
Effective Output Capacitance Energy Related (Note 3)	$C_{O(ER)}$		12		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related (Note 4)	$C_{O(TR)}$		18		pF	
Total Gate Charge	Q_G		0.7		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		0.2		nC	
Gate-to-Drain Charge	Q_{GD}		0.2		nC	
Output Charge	Q_{OSS}		7.3		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	
Output Capacitance Stored Energy	E_{OSS}		0.94		µJ	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Performance Graphs

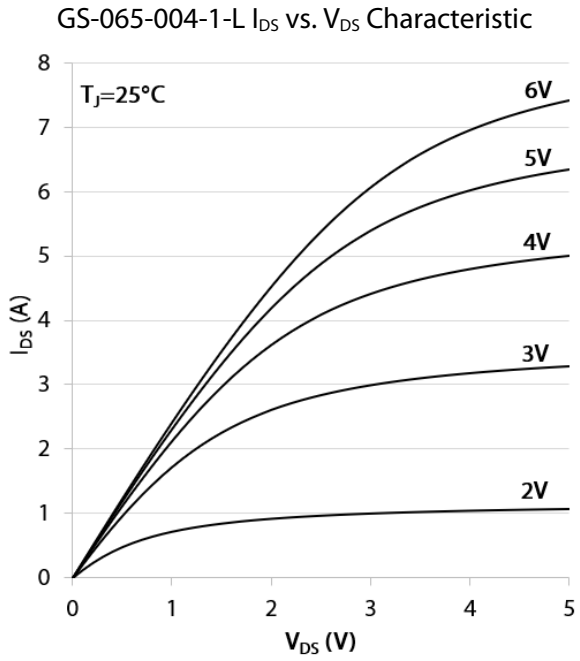


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

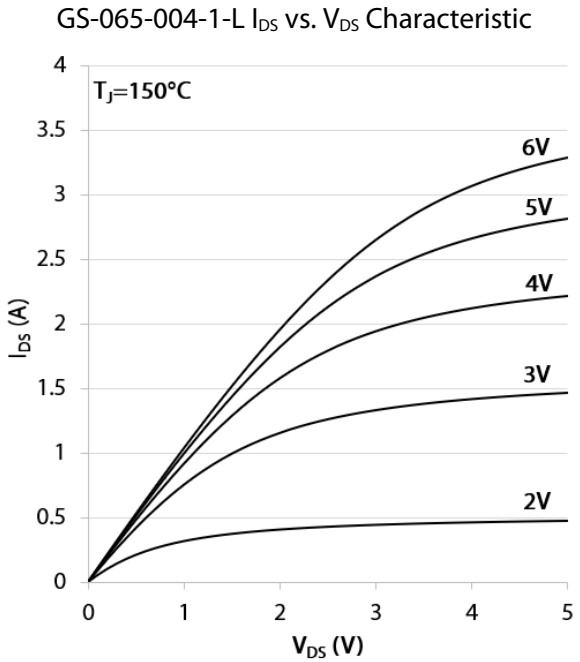


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

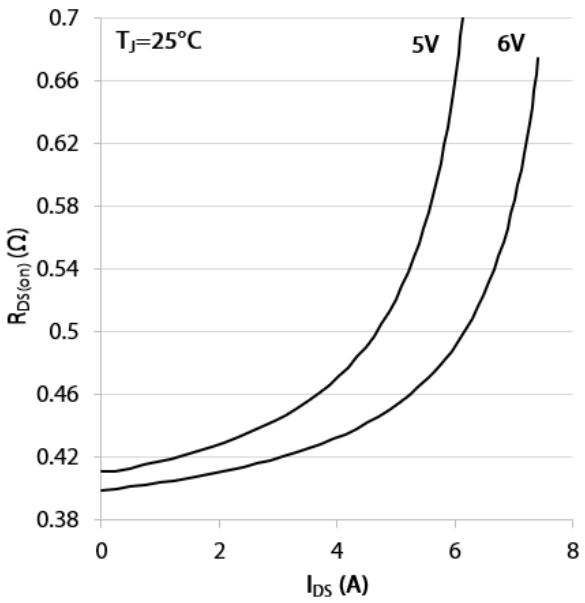


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

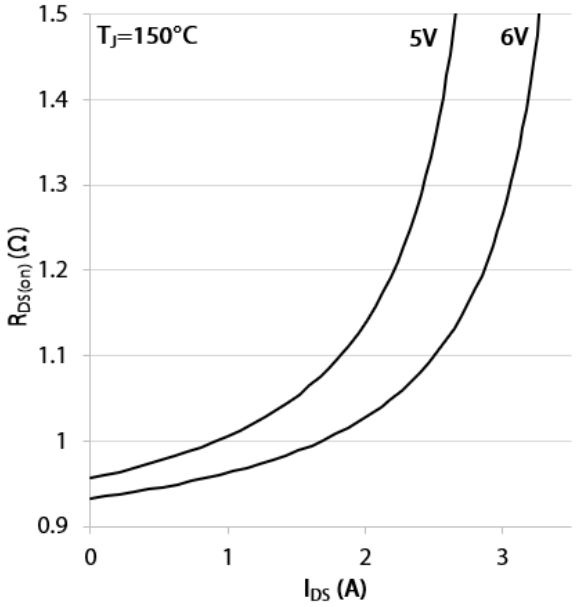


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

GS-065-004-1-L I_{DS} vs. V_{DS}, T_J dependence

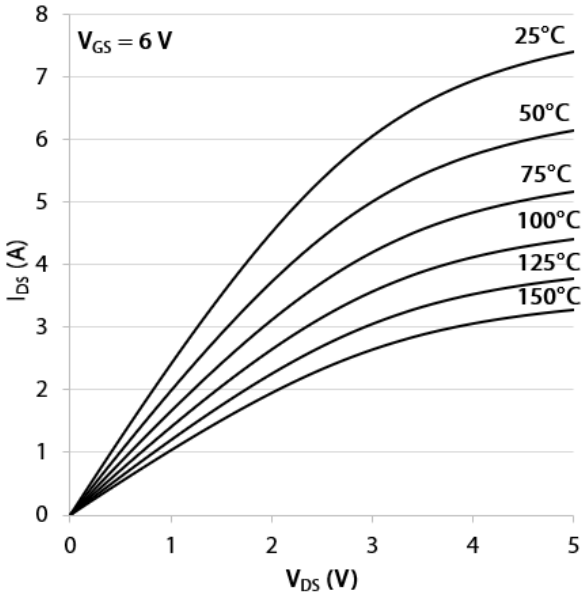


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

GS-065-004-1-L Gate Charge, Q_G Characteristic

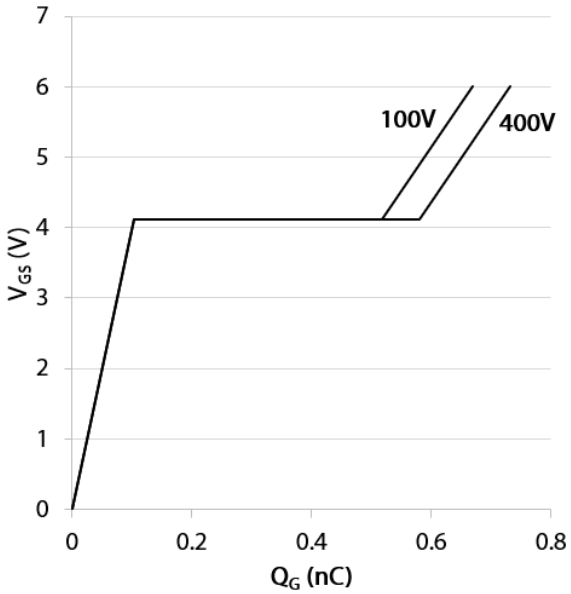


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 100, 400 V

GS-065-004-1-L Capacitance Characteristics

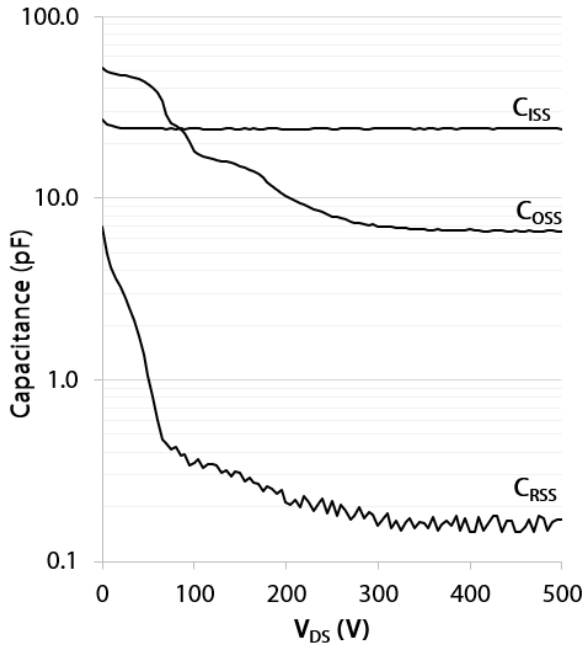


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

GS-065-004-1-L Stored Energy Characteristic

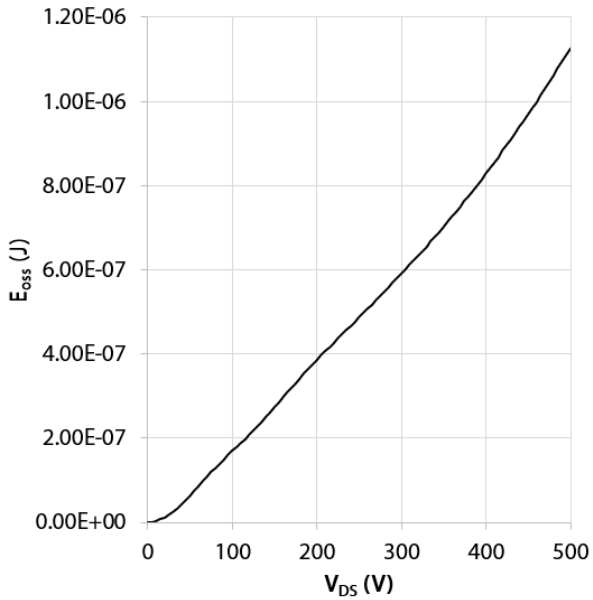


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

GS-065-004-1-L Reverse Conduction Characteristics

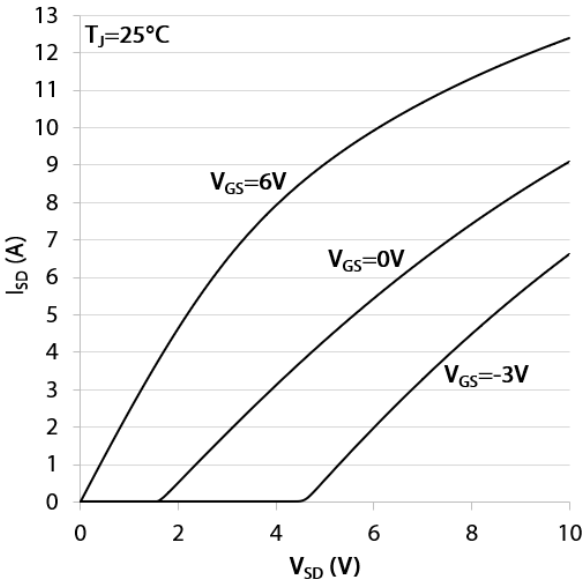


Figure 9: Typical I_{SD} vs. V_{SD}

GS-065-004-1-L I_{DS} vs. V_{GS} Characteristic

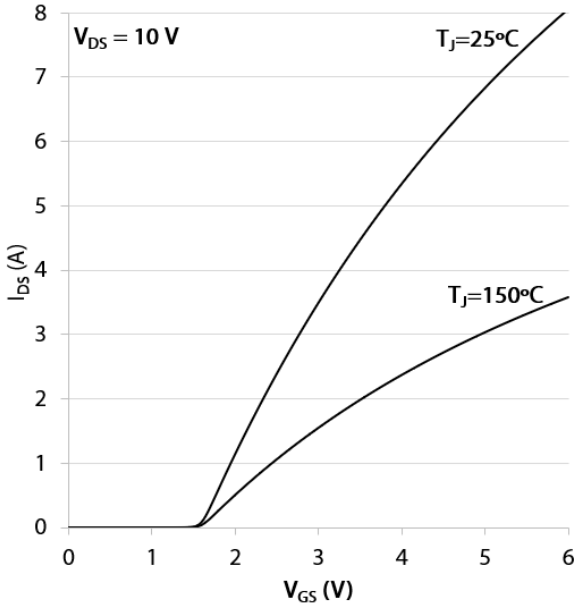


Figure 10: Typical I_{DS} vs. V_{GS}

$R_{DS(on)}$ Temperature Dependence

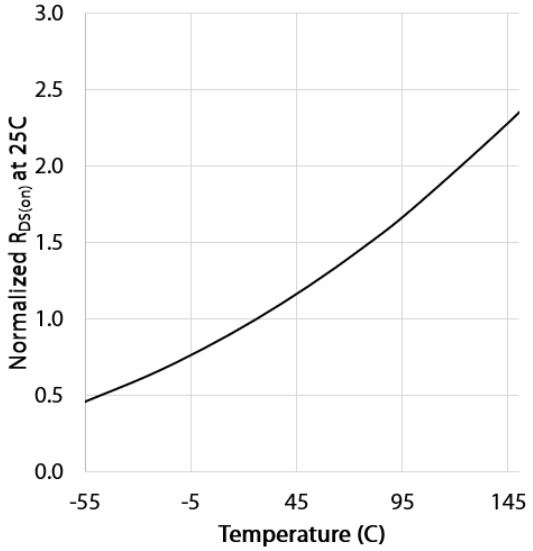


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

GS-065-004-1-L I_{DS} - V_{DS} SOA

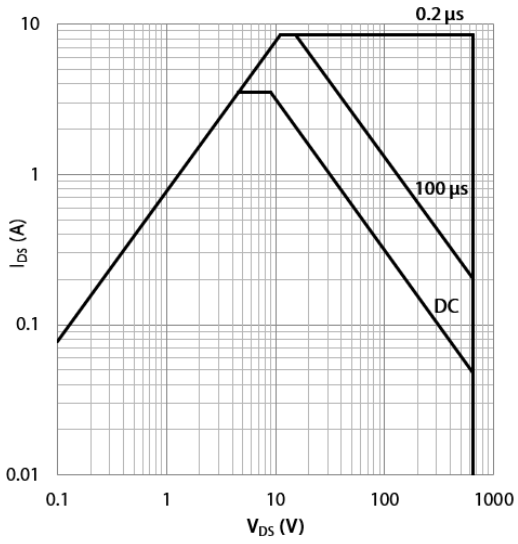


Figure 12: Safe Operating Area @ T_{case} = 25 °C

Thermal Performance Graphs

GS-065-004-1-L Power Dissipation
Temperature Derating

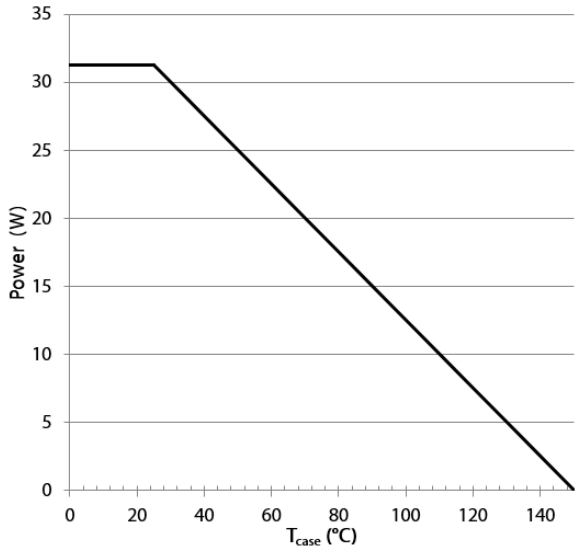


Figure 13: Power Derating vs. T_{case}

GS-065-004-1-L Transient $R_{\theta JC}$

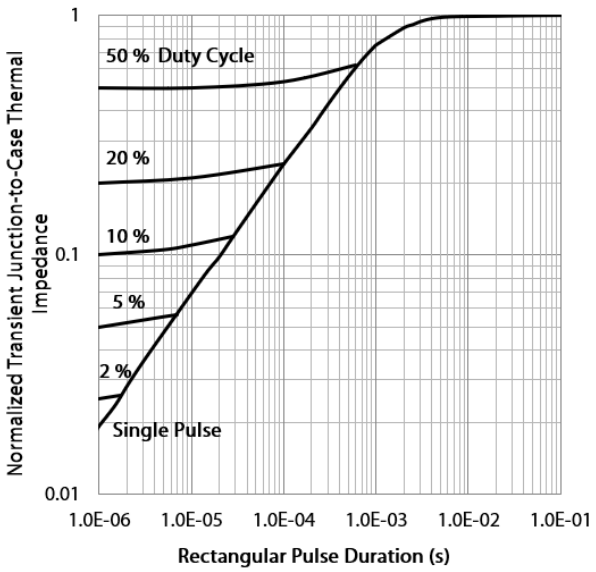


Figure 14: Transient Thermal Impedance
1.00 = Nominal DC thermal impedance

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001" at www.gansystems.com.

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

The GS-065-004-1-L has a dedicated source sense pin. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved connecting the gate drive signal from the driver to the gate pad on the GS-065-004-1-L and returning from the source sense pad on the GS-065-004-1-L to the driver ground reference.

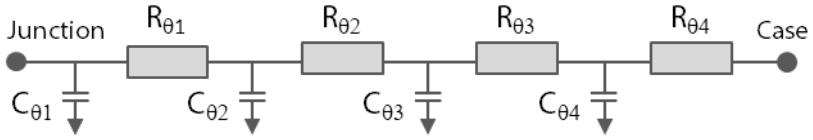
Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the GS-065-004-1-L. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

GS-065-004-1-L RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.2	$C_{\theta 1}$ = 1.1E-05
$R_{\theta 2}$ = 2.4	$C_{\theta 2}$ = 8.0E-05
$R_{\theta 3}$ = 1.3	$C_{\theta 3}$ = 8.0E-04
$R_{\theta 4}$ = 0.1	$C_{\theta 4}$ = 1.0E-03

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*™ Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $V_{(BL)DSS}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated $V_{(BL)DSS}$. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for 1 µs is acceptable.

Packaging and Soldering

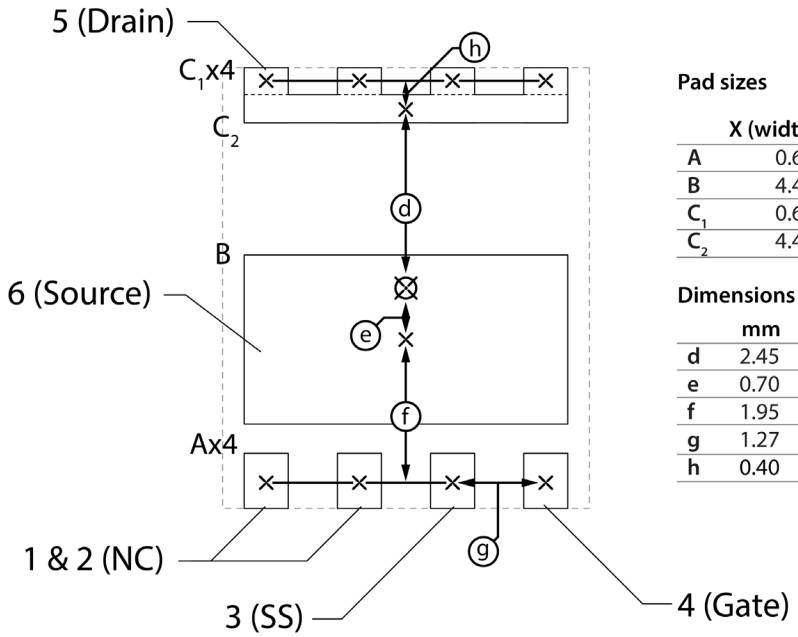
The package is a standard PDFN and it can handle at least 3 reflow cycles.

The recommended reflow profile for Pb-free SAC305 assembly is as below (measured on the part):

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Max peak temperature is 250 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 C it is recommended to also clean the "Non-Clean" paste residues.

Recommended PCB Footprint



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	0.60	0.80	0.024	0.031
B	4.41	2.30	0.174	0.091
C_1	0.60	0.40	0.024	0.016
C_2	4.41	0.40	0.174	0.016

Dimensions

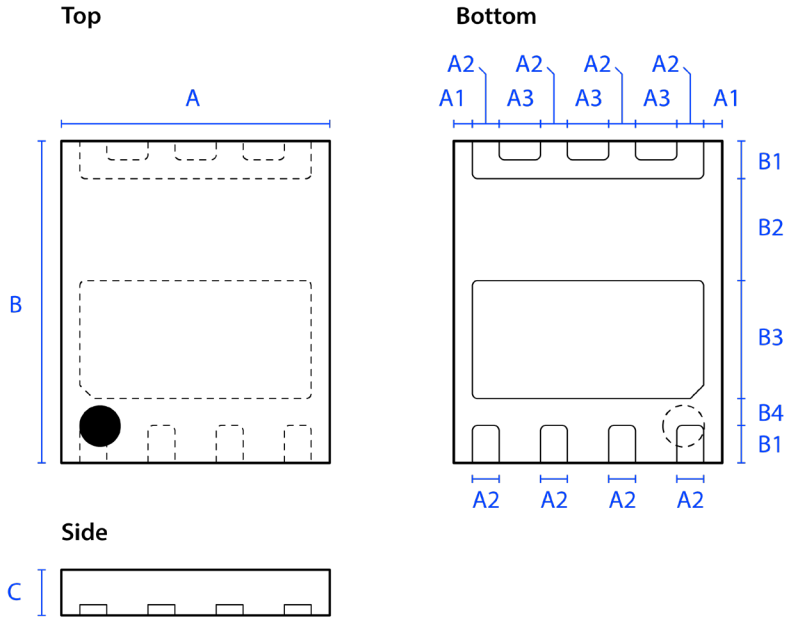
	mm	Inches
d	2.45	0.096
e	0.70	0.028
f	1.95	0.077
g	1.27	0.050
h	0.40	0.016

PCB pad openings

Package outline

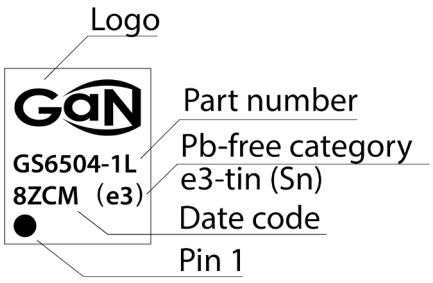
Top side view

Package Dimensions

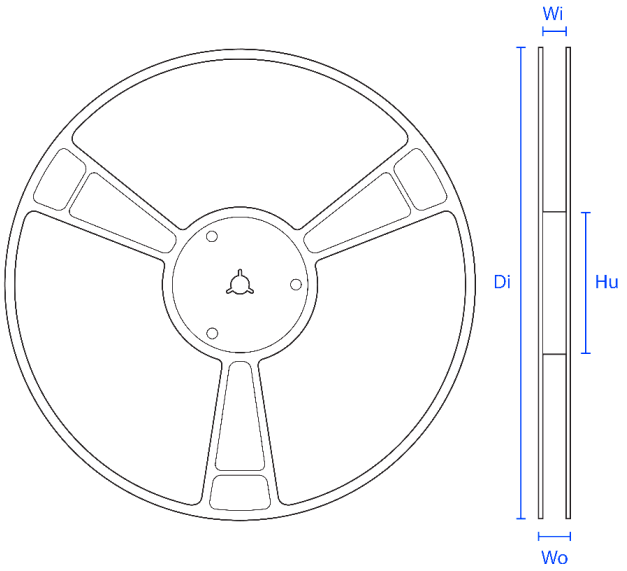


Dimensions (mm)	Min	Max
A	4.90	5.10
A1	0.245	0.445
A2	0.40	0.60
A3	0.67	0.87
B	5.90	6.10
B1	0.60	0.80
B2	1.80	2.00
B3	2.10	2.30
B4	0.40	0.60
C	0.75	0.95

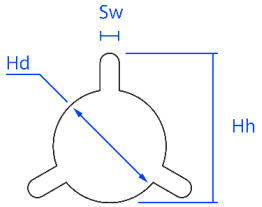
Part Marking



GS-065-004-1-L Reel Information

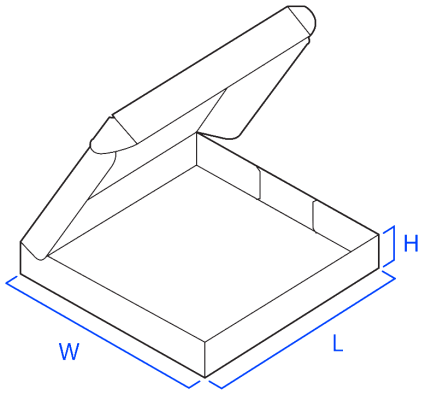


Dimensions (mm)		
7″ mini-reel (180 mm)		
	Nominal	Tolerance
Di	180.0	+0.0 / - 3.0
Wo	18.4	MAX
Wi	12.4	+ 2.0 / - 0.0
Hu	55.0	+/- 5.0
Hh	16.6	+5.0 / - 0.2
Sw	1.6	MIN
Hd	13.0	+5.0 / - 0.2



Note: Wo and Wi measured at hub

Tape and Reel Box Dimensions



Outside dimensions (mm)	
	7″ mini-reel
W	205
L	203
H	35