

Loss Distribution among Paralleled GaN HEMTs

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Abstract— The market and opportunities are growing for GaN HEMTs in high-power applications. In many cases, GaN HEMTs need to be paralleled to increase the power capability or to enhance the efficiency. Unbalanced loss distribution among paralleled switches could cause overtemperature issues potentially, which will result in the derating of the power stage or even cause system failure. An analytical loss model is derived to analyze the tolerance of device characteristics variation for parallel. An auto-balancing mechanism for both switching loss and conduction loss is observed with paralleled GaN HEMTs due to the negative temperature coefficient of transconductance in the whole operating range. Stable operation is expected under all conditions without preselecting GaN HEMTs for parallel. Metal-core PCB based 240A/650V power modules are built with randomly selected GaN HEMTs and tested under high-power conditions. The junction temperatures of paralleled GaN HEMTs are measured to monitor the loss distribution, and the characteristic of GaN HEMTs in parallel is verified.

Keywords—GaN HEMT; paralleling; loss distribution

I. INTRODUCTION

GaN HEMT has been a focus in both academia and industry, due to the ultra-fast switching transitions and extremely low figure of merits ($R_{DS(on)} \times Q_G$), compared with conventional Silicon counterparts. The market and opportunities of GaN HEMTs are growing in automotive and industrial applications, e.g., inverters, onboard electrical vehicle charger, energy storage system, and so on.

The largest GaN transistor GaN Systems' 650V / 13 mOhm bare die (GS-065-120-1-D) has been commercially available. However, in many cases, GaN HEMTs still need to be paralleled to increase the system power capability or to enhance the system efficiency. How to parallel GaN HEMTs reliably and efficiently is a very practical topic to explore.

Due to the ultra-fast transition, the switching performance of GaN HEMTs are very sensitive to circuitry parasitics. In the previous works [1][2][3][4], the effects of parasitic parameters on have been thoroughly analyzed. In [2], a half-bridge power stage with four 650V/60A GaN HEMTs in parallel is prototyped and evaluated with double pulse test under 400V/240A. Reliable hard switching-on and switching-off transitions have been realized without slowing down or derating the GaN HEMTs. The conclusion could be clearly drawn that reliable hard switching on and off transition could be realized by paralleled GaN HEMTs.

On the other hand, the loss distribution among the paralleled GaN HEMTs is another important aspect to consider for the sake of system efficiency and reliability. Overtemperature caused by

unbalanced loss sharing in the power stage will derate the devices, affect system reliability, or even cause system failures.

The static loss, i.e. conduction loss distribution is determined by the temperature dependency of device forward voltage drop. The importance of positive temperature coefficient of semiconductor conduction loss is well addressed by both industry and academia. The $R_{DS(on)}$ of GaN HEMTs has shown an obvious positive dependency on temperature as Si MOSFETs and IGBTs. In parallel applications, the junction temperature of HEMTs of lower $R_{DS(on)}$ devices will increase to balance the current sharing during on-state.

However, is this enough for an even loss distribution among paralleled transistors? In many high voltage and high frequency applications, even though the wide band-gap devices are employed, the switching loss could be similar to, or even higher than the conduction loss. In these cases, the switching loss will become very important or even dominant for temperature sharing.

This paper is aimed to evaluate the switching loss distribution among paralleled GaN HEMTs under continuous conditions. The comparison with SiC MOSFET will also be presented.

In section II, an analytical loss model of the switching transition is derived for paralleled GaN HEMTs, based on which the tolerance of device characteristics variation for parallel are quantitatively analyzed. In section III, metal-core PCB based 240A/650V GaN power modules are built and evaluated by a novel full bridge energy storage and recirculating circuit. The junction temperatures of paralleled GaN HEMTs are measured to monitor the loss distribution under different conditions. Section IV is the conclusion.

II. ANALYTICAL SWITCHING LOSS MODEL FOR PARALLELED GAN HEMTS

Instead of trying to predict the exact loss distribution of paralleled transistors, the aim of this section is to understand the effects of parasitics and device characteristics on loss distribution during the switching process via the built analytical model. Numerical methods, e.g. SPICE simulation, will be a more efficient way to precisely model the non-linear transconductance and parasitic capacitance of power switches.

During the switching-off transition as addressed in the previous work[2], the ultra-small parasitic capacitance of GaN HEMTs makes it possible to deplete the two-dimensional electron gas (2DEG) before the dv/dt period. As a result, the switching-off loss of GaN HEMTs is minor. For zero voltage

switching-on (ZVS) applications, the conduction loss usually dominates the overall semiconductor loss.

So, the temperature distribution among paralleled transistors in ZVS applications is quite straightforward: the junction temperature of HEMTs with lower $R_{DS(ON)}$ will increase to balance the static current-sharing during the on-state. Such automatic loss balancing mechanism will result in an even temperature distribution. For this reason, this paper will focus on the hard switching-on applications.

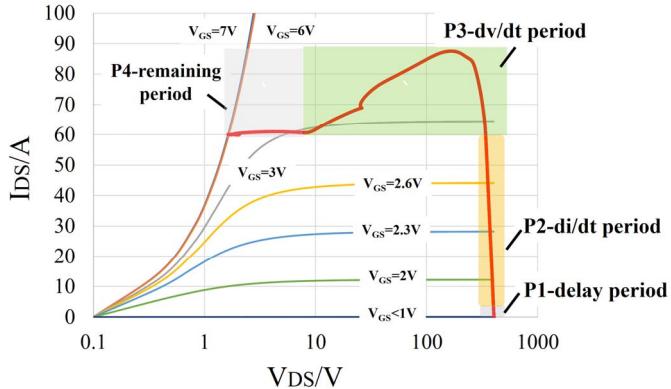


Fig.1. The switching-on process of GaN HEMTs

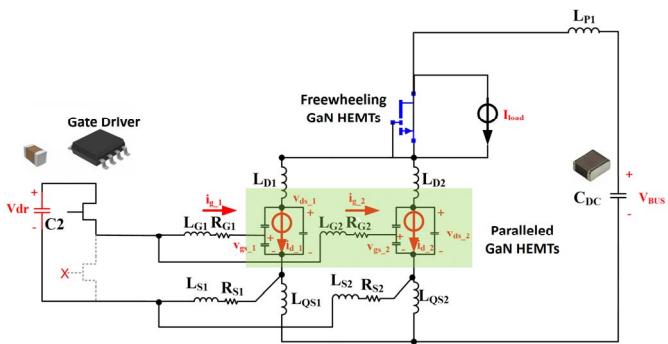


Fig.2 Equivalent circuit of paralleled GaN HEMTs in P2 period

As indicated in the previous work[2][5], the switching-on process of unipolar power switches, e.g.GaN HEMT and MOSFET, could be divided into four periods, P1-delay period, P2-di/dt period, P3-dv/dt period, P4-remaining period as shown in Fig.1. Most of the switching-on loss is generated during P2 and P3 period.

The equivalent circuit of P2-di/dt period is shown in Fig.2. After either of the gate-source voltage of the paralleled HEMTs reaches the threshold voltage (V_{th}), the switch current begins to increase. This period ends when the total 2DEG current reaches the load current. The circuit equations are expressed by (1)~(4)

$$v_{GS_1} = V_{dr} - v_{QS_1} - M_1 \cdot \frac{di_{D_1}}{dt} - R_{G1} \cdot i_{G_1} - L_{G1} \cdot \frac{di_{G_1}}{dt} \quad (1)$$

$$v_{DS_1} = V_{BUS} - L_{P1} \cdot \left(\frac{di_{D_1}}{dt} + \frac{di_{D_2}}{dt} \right) - M_1 \cdot \frac{di_{G_1}}{dt} - (L_{D1} + L_{QS1}) \cdot \frac{di_{D_1}}{dt} \quad (2)$$

$$i_{DS_1} = g_1 \cdot (v_{GS_1} - V_{th1}) \quad (3)$$

$$v_{QS_1} = (L_{QS1} \cdot \frac{di_{D_1}}{dt} - L_{QS2} \cdot \frac{di_{D_2}}{dt}) \cdot \frac{Z_{S2}}{Z_{S1} + Z_{S2}} \quad (4)$$

where g is the transconductance of GaN HEMT, R_{G1} and L_{G1} is the total resistor and inductance of gate driver loop, Z_{S1} and Z_{S2} is the impedance of the Kelvin source senses (L_{S1} , R_{S1} and L_{S2} , R_{S2}), M_1 is the mutual inductance between gate driver loop and power commutation loop.

As shown in Fig.1, the device is operating in the saturation region during the P2 period, so the dynamic current sharing is mainly determined by the gate-source voltage and device characteristics instead of parasitics. Furthermore, according to (1) and (4), the quasi-common source inductance (L_{QS1} and L_{QS2}) will cause a negative feedback voltage (V_{QS1} and V_{QS2}) on V_{GS} to balance the dynamic current. To simplify the analysis, also as a worse case, the circuit parasitics are ignored, so the switching energy during P2 is derived as (5).

$$E_{on1_{P2}} = \int_{R_G C_{iss} \cdot \ln(\frac{V_{dr}}{V_{dr} - V_{th1}})}^{R_G C_{iss} \cdot \ln(\frac{V_{dr}}{V_{dr} - V_{th2}})} g_1 \cdot [V_{dr} \cdot \left(1 - e^{\frac{-t}{R_G C_{iss}}} \right) - V_{th1}] \cdot V_{BUS} dt \quad (5)$$

Here,

$$V_{GS\text{miller}} = \frac{(g_1 \cdot V_{th1} + g_2 \cdot V_{th2}) \cdot C_{RSS} \cdot R_g + I_{Load} \cdot C_{RSS} \cdot R_g + V_{dr} \cdot C_{oss}}{(g_1 + g_2) \cdot C_{RSS} \cdot R_g + C_{oss}}$$

the average value of the gate-source voltage during miller plateau.

Similarly, the switching loss during P3-dv/dt period is derived as

$$E_{on1_{P3}} = \int_0^{I_{LOAD} - g_1(V_{GS\text{miller}} - V_{th1}) - g_2(V_{GS\text{miller}} - V_{th2})} \frac{v_{DS} \cdot I_{LOAD} \cdot i_{DS_1}}{i_{DS_1} + i_{DS_2}} dt + E_{oss} \cdot \frac{g_1(V_{GS\text{miller}} - V_{th1})}{g_1(V_{GS\text{miller}} - V_{th1}) + g_2(V_{GS\text{miller}} - V_{th2})} \quad (6)$$

where E_{oss} is the energy stored on the output capacitance of high-side and low-side transistors.

The threshold voltage and transconductance of GaN HEMTs (GS66516B) at different temperatures are measured by the curve-tracer as shown in Fig.3. Different from SiC MOSFET [8], the threshold voltage of GaN HEMTs is nearly constant as a function of junction temperature. At the same time, an obvious negative dependency of transconductance on temperature is observed.

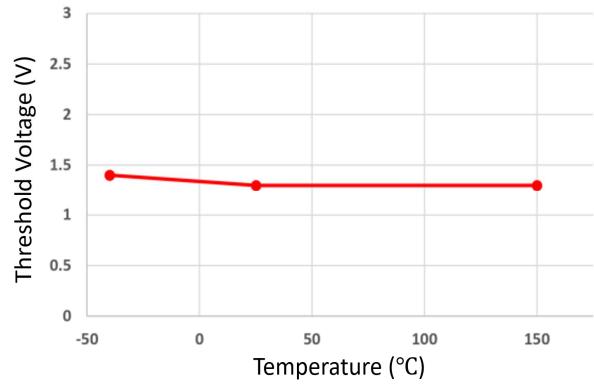


Fig.3.a V_{TH} of GS66516B vs. temperature

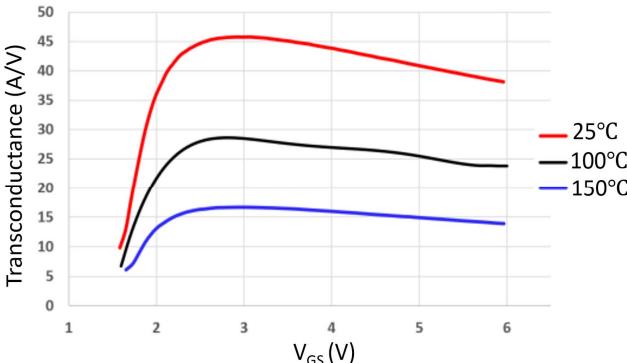


Fig.3.b Transconductance of GS66516B vs. temperature

Higher junction temperature will result in a significantly lower switching loss on GaN HEMTs as shown in Fig.4.a. Such automatic junction temperature balancing mechanism of the switching loss will increase the tolerance for device characteristic variation and system robustness. The junction temperature difference of paralleled GS66516B (assumed thermally isolated, $R_{THJA}=2\text{ }^{\circ}\text{C/W}$) in a 120kHz, 100V/400V, 4kW boost converter is calculated under different characteristic variations as shown in Fig.4.b. The junction temperature difference will be lower than 9°C with randomly selected GaN HEMTs. As shown in Fig.4.c, the switching loss of warming SiC MOSFET will increase, which will result in unbalanced temperature distribution, or even thermal run-away.

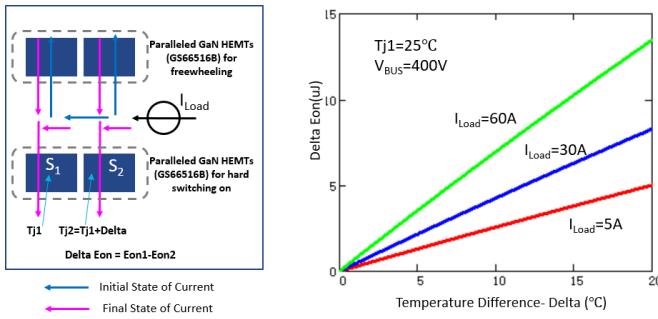


Fig.4.a Delta Eon vs. Delta T among Paralleled GaN HEMTs

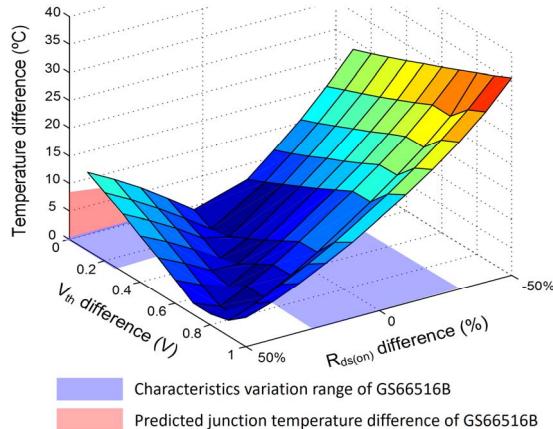


Fig.4.b Delta T vs. Characteristics variation

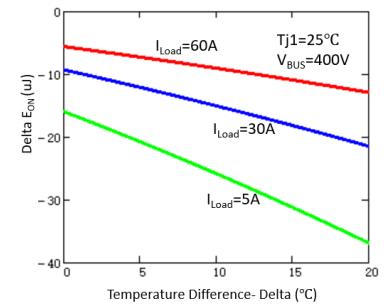
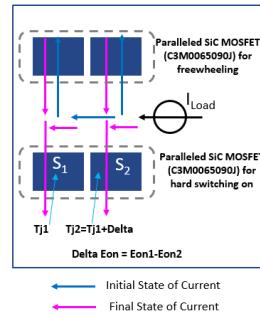


Fig.4.c Delta Eon vs. Delta T among Paralleled SiC MOSFET

III. TEST SETUP AND GAN POWER MODULE UNDER TEST

In this paper, the junction temperatures of paralleled GaN HEMTs will be measured to verify the loss distribution. The thermal conduction path of each GaN HEMT on the insulated metal substrate is shown in Fig.5 [9][10]. According to the FEM simulation results, transistors are nearly thermally insulated, which makes IMS a ideal substrate for this experiment.

As shown in Fig.6, two IMS-based half-bridge power modules consisting of four high-side and four low-side 60A / 650V GaN HEMTs in parallel are configured as a full power emulation circuit to experimentally verify GaN HEMT's automatic balancing effect of switching loss on junction temperature distribution. GaN HEMTs are randomly picked to build the power modules, whose static test results (V_{th} and $R_{ds(on)}$) are shown in Fig.7.

The operating rule of the full power emulation circuit is described in [11]. Combining frequency varying and phase shifting control, the energy is able to be recirculated inside the circuit emulating the high-power conditions for device under test.

In the hard switching mode, the switching frequency of the hard switching-on leg (S_1 and S_2) is five times of the soft switching-on leg (S_3 and S_4). Inside each leg, the operation of high side and low side switches is symmetrical. In every period, two hard switching-on transitions and three hard switching-off transitions happen on the transistors of the hard switching-on leg; two hard switching-off transitions happen on transistors of soft switching-on leg.

The automatic balancing effect of $R_{ds(on)}$ with positive temperature coefficient is straightforward and well addressed by the industry. To ensure the domination of the switching-on loss and to minimize the effect of $R_{ds(on)}$, 1MHz switching frequency (hard-switching leg) is applied.

The waveform and temperature distribution at $I_{max}=52\text{A}$ are shown in Fig.8.a. Junction temperatures of paralleled transistors at different current are shown in Fig.8.c. Good thermal balance is achieved with randomly-selected GaN HEMTs.

The junction temperature difference is 11°C for the worst case, and <1°C for the best case. Combined with the static test results shown in Fig.7, it is clear that the threshold voltages determine the temperature distribution at 1 MHz.

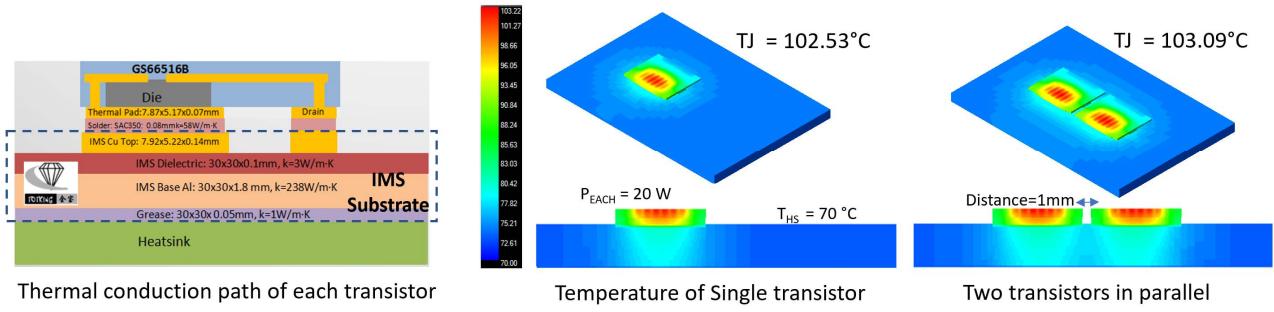


Fig.5 Thermal finite element analysis (FEM) simulation results of GaN HEMTs on the IMS substrate

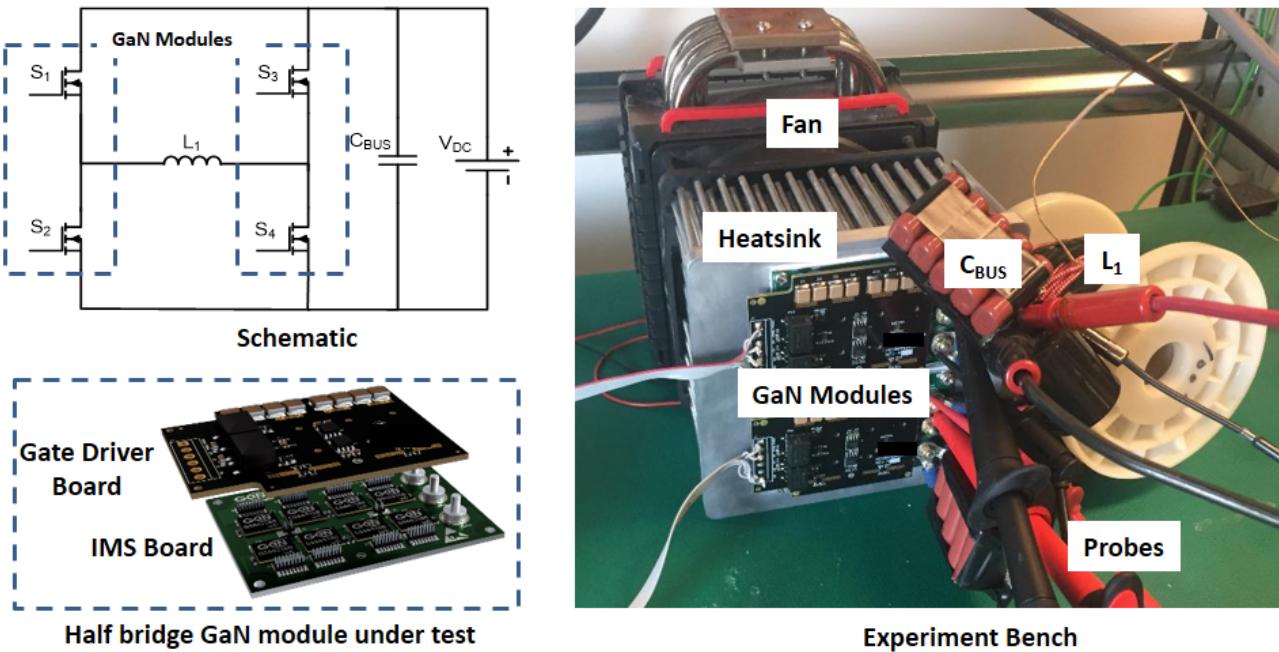


Fig.6 Power modules under test and the full power emulation circuit

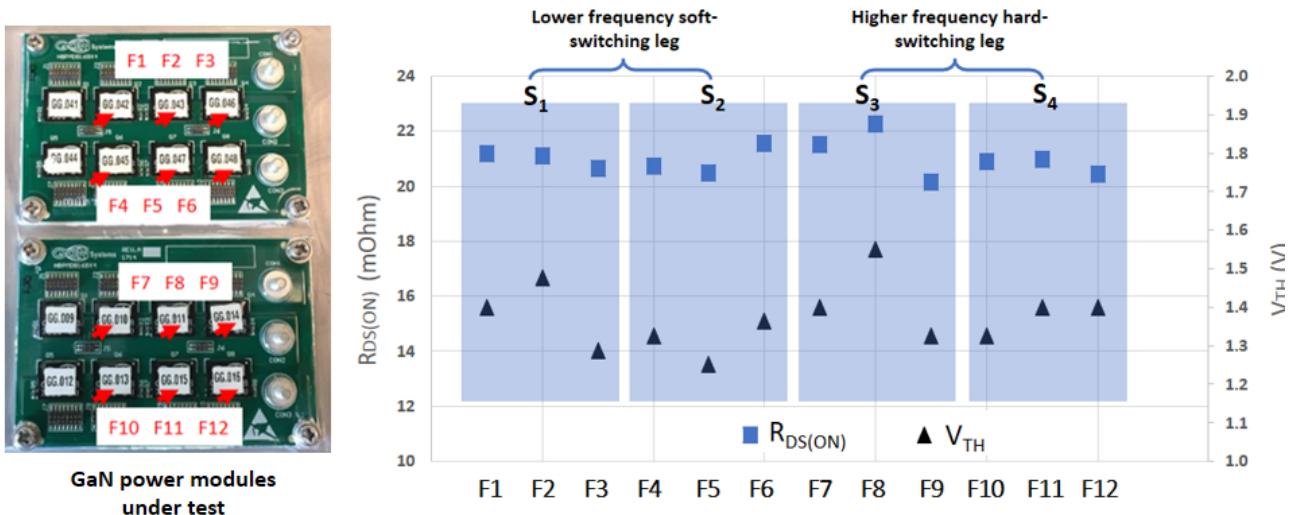


Fig.7 Static test results of paralleled GaN HEMTs

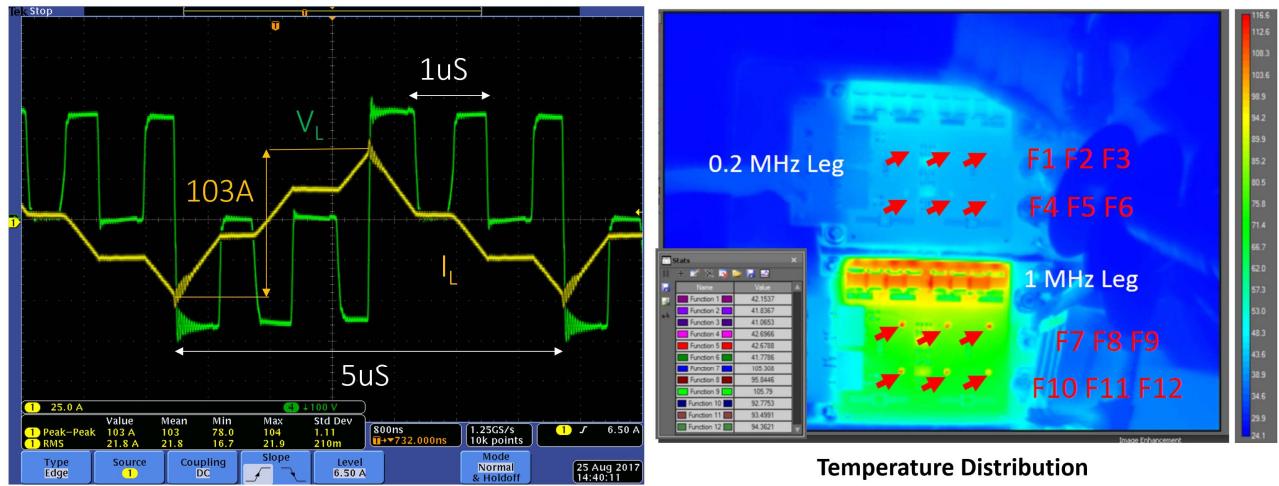


Fig.8.a Experimental waveforms and temperature distribution at 1 MHz

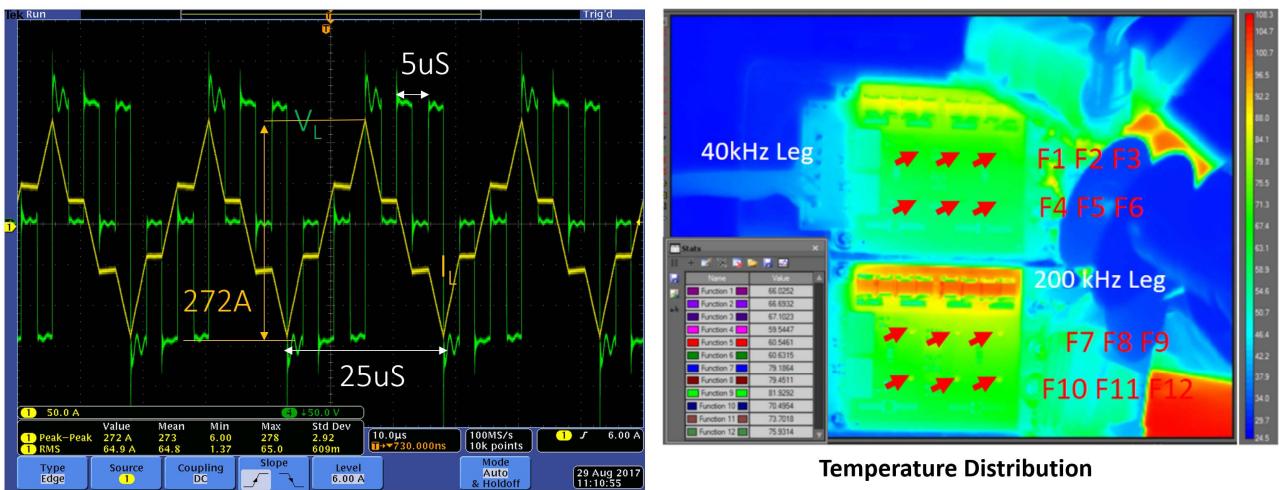


Fig.8.b Experimental waveforms and temperature distribution at 200 kHz

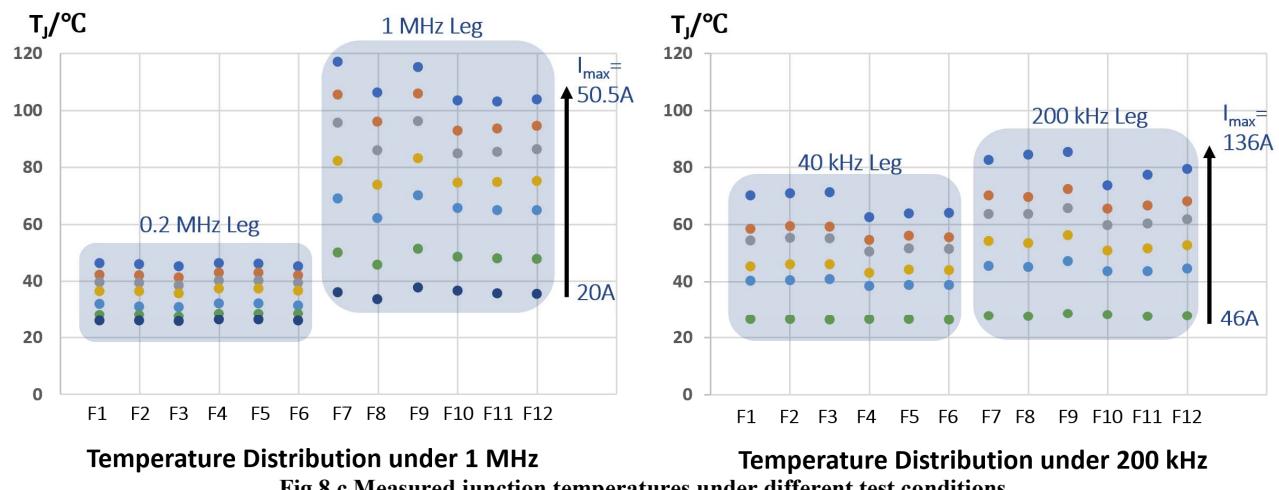


Fig.8.c Measured junction temperatures under different test conditions

The experimental waveform and temperature distribution at 200 kHz, a more practical switching frequency for such high-power hard switching applications, are shown in Fig.8.b. The junction temperatures are recorded in Fig.8.c. The junction temperature difference is $<6^{\circ}\text{C}$ for the worst case, $<3^{\circ}\text{C}$ for the best case. The $R_{\text{DS(ON)}}$ begins to affect the temperature distribution @ 200kHz.

IV. CONCLUSION

In this paper, an analytical model of switching-on loss of paralleled GaN HEMTs is derived, and the factors for loss sharing is quantitatively analyzed. Due to the negative feedback mechanism between junction temperature and both and switching loss and conduction loss of GaN HEMTs, the thermal runaway is less likely to happen in paralleling applications.

Moreover, a 240A/650V half-bridge power module with IMS substrate is built with randomly selected GaN HEMTs. A full power emulation platform is employed to test GaN power modules under different switching frequency. Excellent junction temperature balancing for paralleled GaN HEMTs is observed.

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