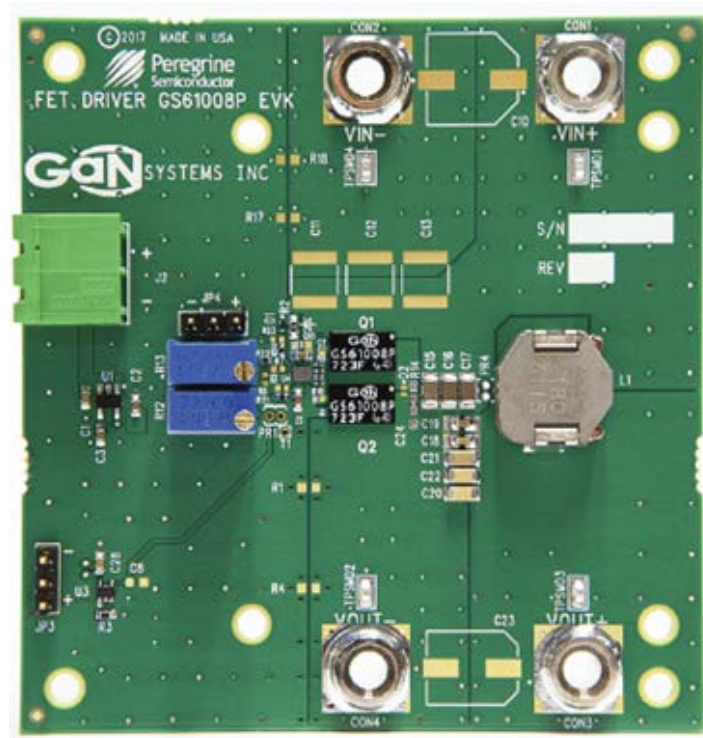


GS61008P-EVBHF

100V GaN E-HEMT Half Bridge Evaluation Kit

User's Guide



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**DANGER!**

Electrical Shock Hazard - Hazardous high voltage may be present on the board during the test and even brief contact during operation may result in severe injury or death. Follow all locally approved safety procedures when working around high voltage.

Never leave the board operating unattended. After it is de-energized, always wait until all capacitors are discharged before touching the board.

This board should be handled by qualified personnel ONLY.



PCB surface can become hot. Contact may cause burns. Do not touch!

**CAUTION:**

This product contains parts that are susceptible to damage by electrostatic discharge (ESD) or exposure to voltages in excess of the specified voltage. Always follow ESD prevention procedures when handling the product. Avoid applying excessive voltages to the power supply terminals or signal inputs or outputs

Introduction

The GS61008P-EVBHF Evaluation Board (EVB) allows the user to evaluate GaN Systems' GS61008P Enhancement Mode High Electron Mobility Transistors (E-HEMTs) with the high-speed Psemi PE29101 gate driver in a half-bridge configuration. The PE29101 integrated high-speed driver is designed to control the gates of GaN Systems' E-HEMTs. The outputs of the PE29101 are capable of providing switching transition speeds in the sub nano-second range. The EVB is controlled by an independent PWM signal, so the half-bridge topology is intended to be used as a power stage for a buck converter.

Evaluation Board Contents and Requirements

Kit Contents

The GS61008P-EVBHF includes the following hardware.

Table 1 • GS61008P-EVBHF Evaluation Kit Contents

Quantity	Description
1	GS61008P-EVBHF GaN E-HEMT evaluation board assembly

Hardware Requirements

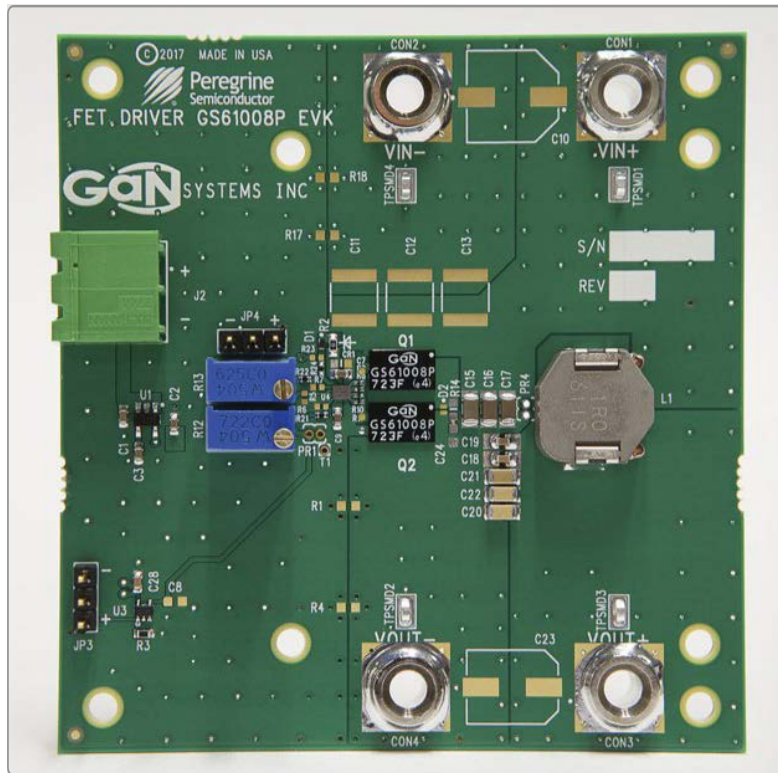
In order to evaluate the performance of the evaluation board, the following equipment is required:

- High speed digital oscilloscope
- Function generator (PWM)
- High voltage DC power supply
- Low voltage DC power supply
- DC test leads

Evaluation Board Assembly Overview

The evaluation board is assembled with a PE29101 gate driver and two GS61008P GaN E-HEMTs. Headers are included for signal input, signal output, and power connections, and probe points are included for waveform measurements.

Figure 1 • GS61008P-EVBHF Half-Bridge Evaluation Board Assembly



Block Diagram and Schematic

The block diagram and schematic of the evaluation board are provided in Figure 2 and Figure 3.

Figure 2 • GS61008P-EVBHF Evaluation Board Block Diagram

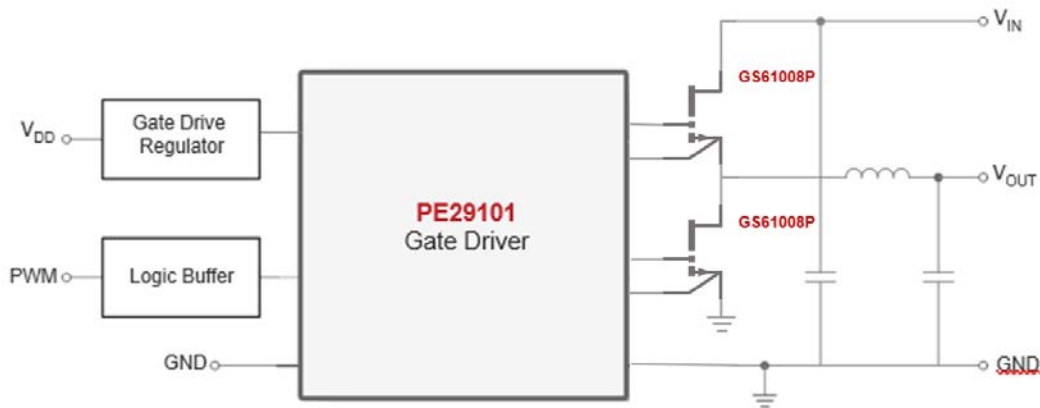
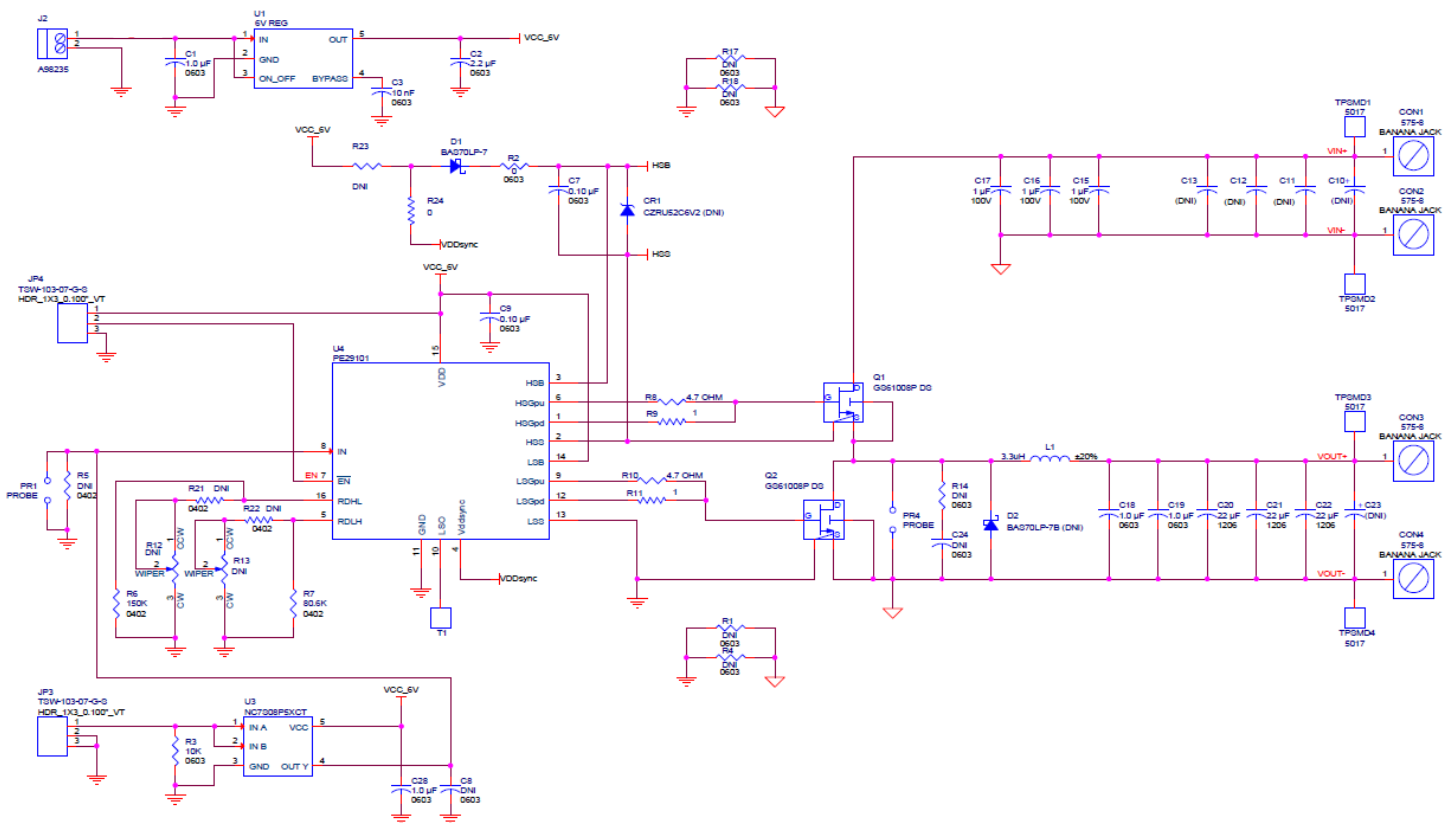


Figure 3 • GS61008P-EVBHF Evaluation Board Schematic



Circuit Description

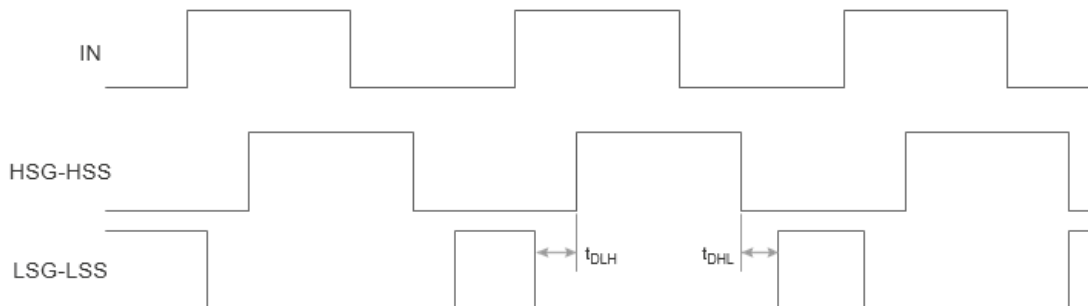
The EVB is assembled with a PE29101 gate driver (U4) and two GS61008B GaN E-HEMTs (Q1 and Q2) in a half-bridge configuration. The PWM input signal is buffered by 2-Input AND gates (U3). Both U3 and U4 are supplied by a 6V regulator (U1). Gate resistors R8–R11 dampen unwanted ringing on the transistor gates by offsetting the parasitic inductance in the gate loop. R14 and C24 form an optional RC snubber to further reduce the slew rate of the switch node voltage, but will increase power losses. The 3.3 μ H inductor is composed of metal alloy, exhibiting low loss with an absolute maximum voltage of 50V.

The PE29101 features an internal dead-time controller that allows the user to minimize the dead time between one transistor turning off and the other turning on. This eliminates any large shoot-through currents, which could dramatically reduce the efficiency of the circuit and potentially damage the transistors.

The dead-time resistors only affect the low-side gate (LSG) output; the high-side gate (HSG) output will always equal the duty-cycle of the input. The HSG will track the duty cycle of the PWM input with a shift in the response, as both rising and falling edges are shifted in the same direction. The LSG duty cycle can be controlled with the dead-time resistors as each resistor will move the rising and falling edges in opposite directions. R6 will change the dead-time from HSG falling to LSG rising and R7 will change the dead-time from LSG falling to HSG rising.

The PE29101 includes an internal synchronous bootstrap protection circuit designed to limit overcharging of the bootstrap capacitor during reverse body diode conduction. Pin 4 (VDDSYNC) of the PE29101 is connected to an external Schottky bootstrap diode, with fast recovery time to protect the die from high voltage.

Figure 4 • PE29101 Dead-time Waveforms



Quick Start Guide

This chapter will guide the user through the evaluation board overview, hardware operation, test setup and test results.

Evaluation Board Overview

The evaluation board contains:

- Header pins for power supply and PWM connection
- Test points for performance verification

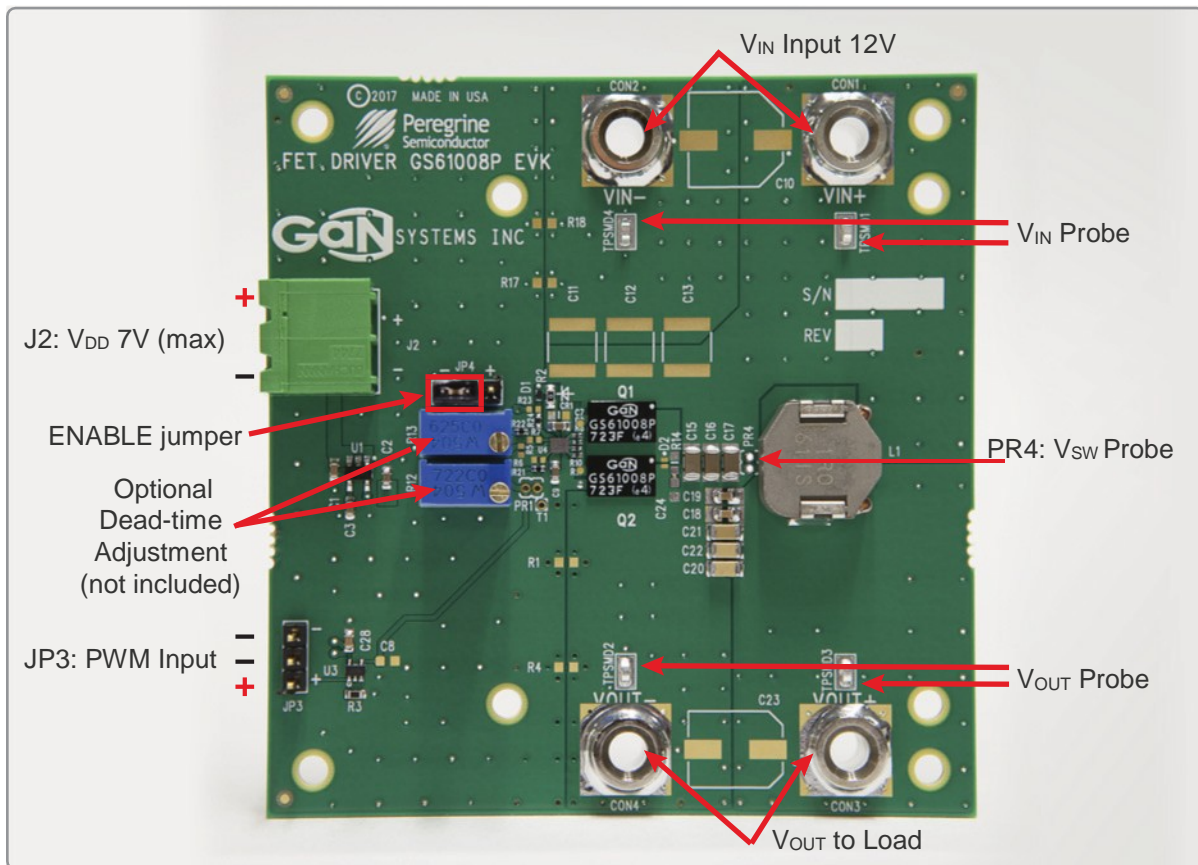
The operating specifications of the evaluation board are as follows:

- Maximum input operating voltage of 50V. (maximum voltage is limited to 50V based on inductor selection, but can be increased to 70V¹ using an inductor with a higher voltage rating)
 - Maximum output current of 12A continuous²
 - Frequency of operation of 0.1 - 5 MHz.
 - Minimum high-side output pulse width of 3 ns (typ.)
 - Minimum low-side output pulse width of 3 ns (typ.)
1. 70V is the reverse voltage rating of the bootstrap diode.
 2. Maximum load current depends on die temperature and is further subject to switching frequency and operating voltage. Forced air cooling or heat sinking can increase current rating.

Evaluation Test Setup

Figure 5 shows the test setup for the GS61008P-EVBHF evaluation board. Make sure that the specified safety precautions mentioned in “Safety Precautions” on page 2 are followed.

Figure 5 • GS61008P-EVBHF Evaluation Board Test Setup



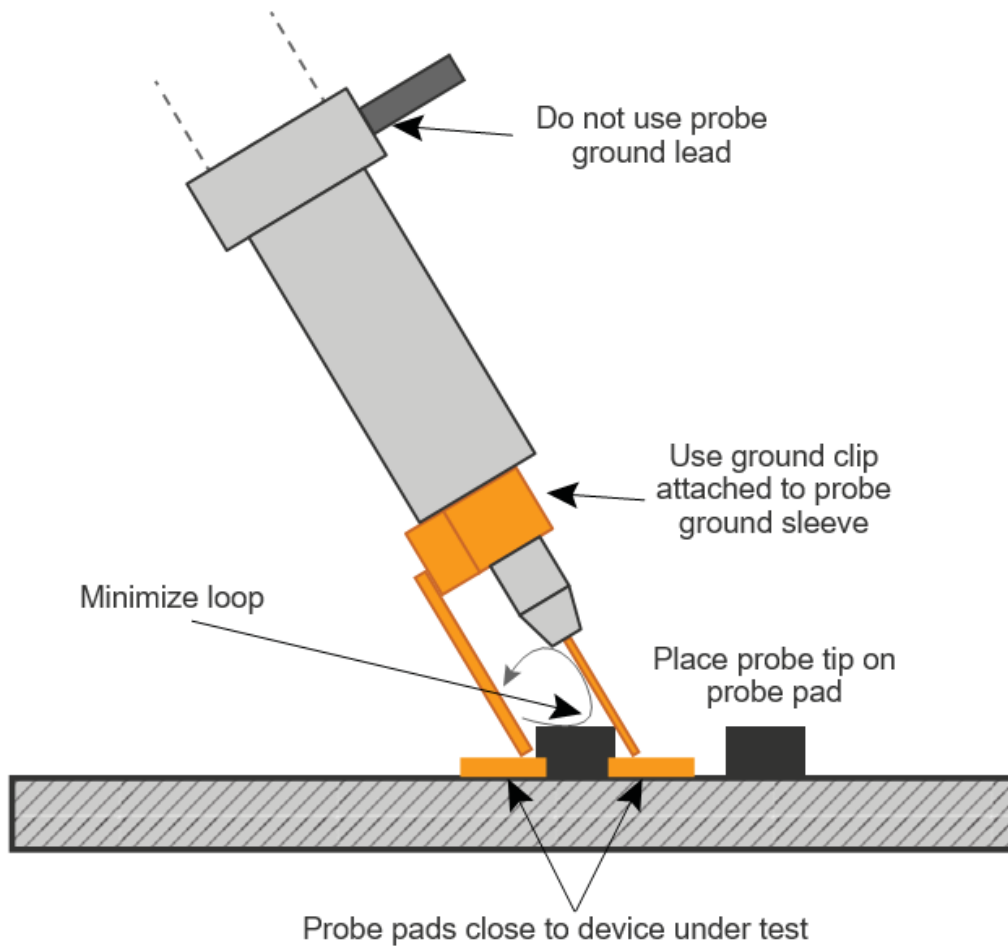
Hardware Operation

The general guidelines for operating the evaluation board are listed in this section. Follow the steps to configure the hardware properly.

- 1) Verify that all DC power supplies are turned off before proceeding.
- 2) Connect the low voltage power supply to J2.
- 3) Apply 7 VDC (max) to J2 to power the PE29101 driver.
- 4) Connect the input PWM control signal to JP3.
- 5) Set the function generator output impedance to 50Ω and supply a pulse output of 2 to 5 VPP (max) and 0V (min). Start with 25% duty cycle at a frequency of 1 MHz.
- 6) Connect the high voltage power supply bus to CON1 (V_{IN+}) and CON2 (V_{IN-}).
- 7) Apply 48V to CON1 (V_{IN+}) and CON2 (V_{IN-}). Do not to exceed the maximum input voltage.
- 8) Connect V_{OUT} to a DC load at CON3 (V_{OUT+}) and CON4 (V_{OUT-}).
- 9) Once operational, adjust the PWM duty cycle to achieve the required output voltage and observe the output switching behavior at test point PR4. Refer to **Figure 6** and **Figure 7**.
- 10) The electronic load can now be applied. Note that as switching frequency and output load increase, care must be taken not to exceed the junction temperature of the devices.
- 11) Dead-time resistors R6 ($150k\Omega$) and R7 ($80.6k\Omega$) are set to maximize efficiency. Optionally, R6 and R6 can be removed and R12 and R13 can be inserted to adjust the dead-time. Setting the potentiometers fully CW will result in minimum dead-time. Note that R21 and R22 ($30k\Omega$) prevent the dead-time resistance from reaching 0 ohms and causing shoot-through.
- 12) Follow the above steps in reverse to power down the evaluation board.

Note: When measuring the high frequency content switch node, care must be taken to avoid long ground leads. Measure the switch node by placing the oscilloscope probe tip through the PR4 via (designed for this purpose) and grounding the probe directly across the GND terminal provided. See Figure 6 for proper probe technique.

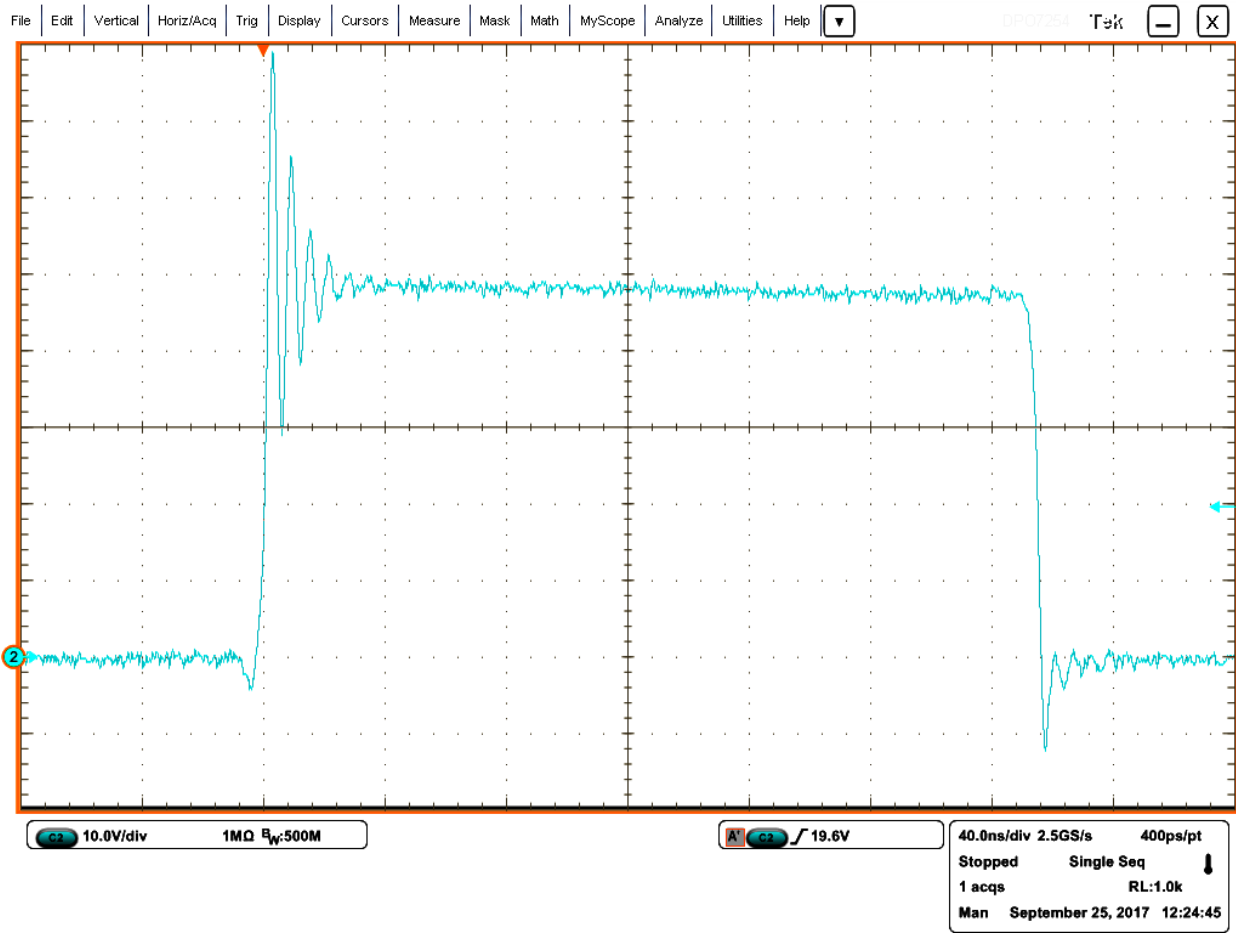
Figure 6 • Proper Oscilloscope Probe Measurement Technique



Evaluation Results

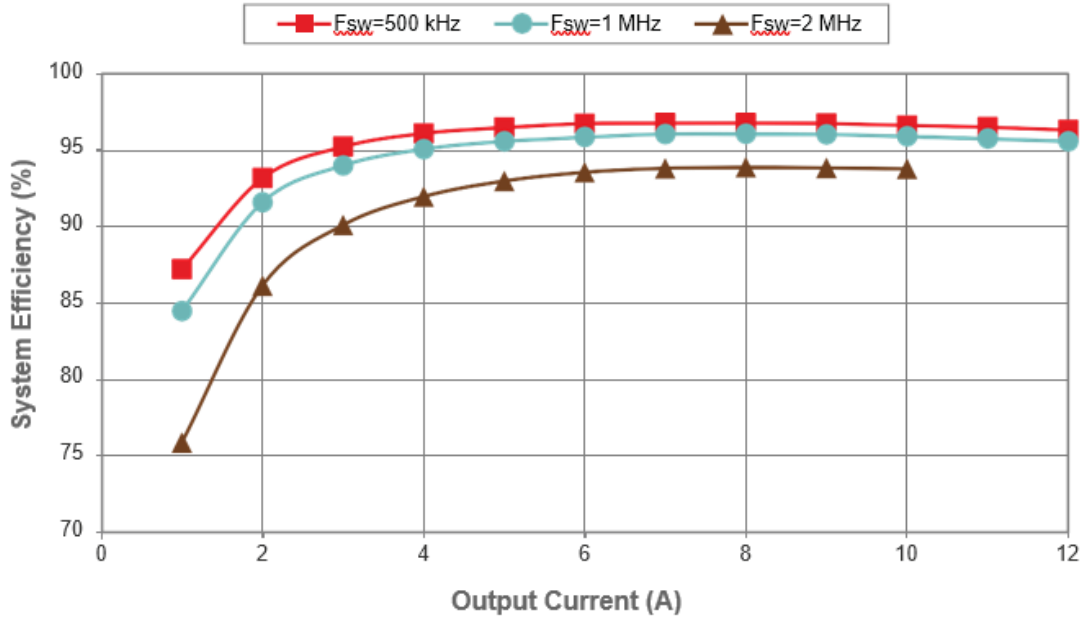
Evaluation results are shown in figures 7 through 9

Figure 7 • Oscilloscope Plot Showing SW Node Signals (*)



- Note: $V_{IN} = 48V$, $V_{OUT} = 12V$, $f_{SW} = 1\text{ MHz}$, $L = 3.3\ \mu\text{H}$, $I_{LOAD} = 10A$

Figure 9 • GS61008P-EVBHF Typical Efficiency ($V_{IN} = 48V$, $V_{OUT} = 12V$, $L = 3.3 \mu H$)



Thermal Considerations

The EVB includes two GS61008P GaN E-HEMTs. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The evaluation board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum junction temperature of +150 °C.

Note: The EVB does not include any on-board current or thermal protection

The thermal performance of the EVB is shown in **Figure 10** and **Figure 11**. The test sample was coated with flat black spray paint to increase the target emissivity to 0.98. Infrared thermography was performed under the following conditions, with no heat sinking, at room-ambient temperature:

- $V_{IN} = 48V$
- $V_{OUT} = 12V$
- $I_{OUT} = 12A$
- $f_{SW} = 1\text{ MHz}$

Figure 10 • GS61008P-EVBHF Evaluation Board ($T_{MAX} = 115.3^{\circ}C$)

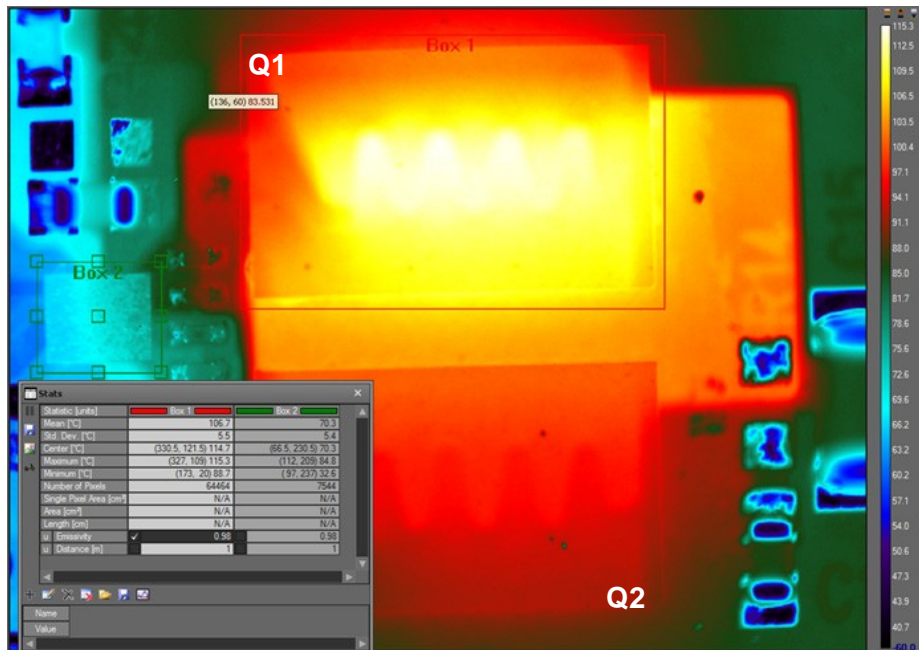
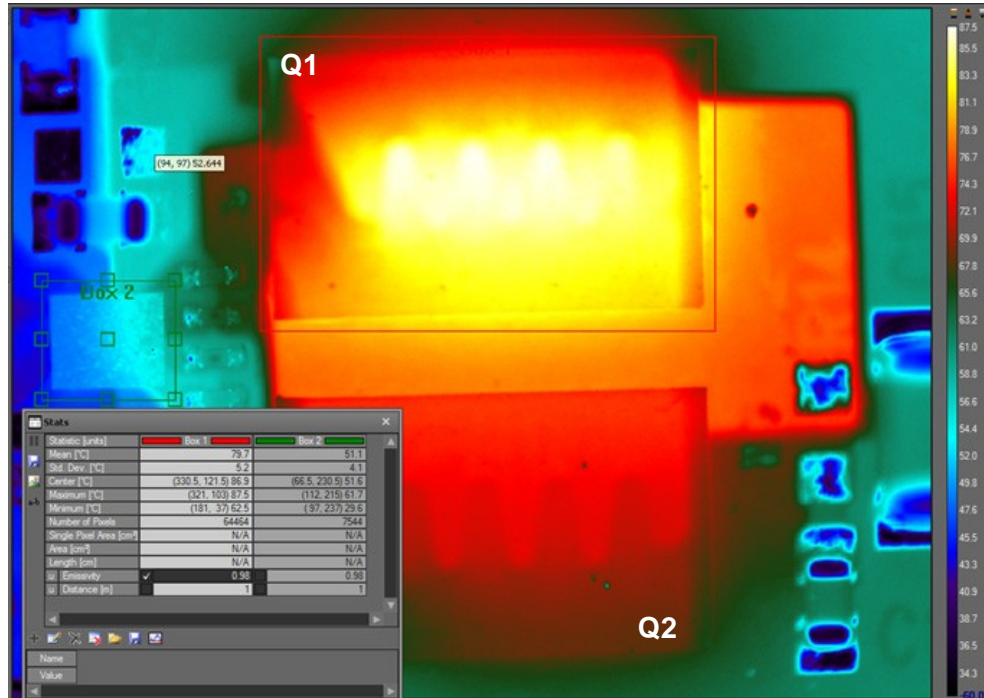


Figure 11 • GS61008P-EVBHF Evaluation Board with Fan On ($T_{MAX} = 87.5^{\circ}\text{C}$)



Technical Resources

This document and additional technical resources are available for download from www.gansystems.com.

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GS61008P-EVBHF Revision History Table

Revision #	Changes from Previous	Owner
180213	First version, based on original document from Psemi. This version was never released	J Ajersch
180227	Changed Peregrine to Psemi plus other minor updates.	J Ajersch
180302	<p>Updates provided by Psemi as highlighted in their document 29101_DOC-85316-1R.pdf</p> <ul style="list-style-type: none"> - Added last sentence in "Introduction" - Added last sentence in paragraph 3 of the "Circuit Description: - Reduced max operating voltage from 80V to 70V - Added "optional" to dead-time adjustment pot description in "Evaluation Test Set Up) - Modified description of how to use dead-time resistors, "item 11 in Hardware Operation" 	J Ajersch
180327	Changed step 5 on page 9. Replaced "Set the function generator output impedance to 50Ω and supply a pulse output of 3 VPP at 1.5V offset." with "Set the function generator output impedance to 50Ω and supply a pulse output of 2 to 5 VPP (max) and 0V (min)" Change based on Psemi's input.	J. Ajersch
180816	Changed input voltage on J2 from 8-12V to 7V (max).	J. Ajersch