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- Layout considerations for paralleling GaN
- Design example of 4x paralleled GaN power stage
- Experimental results
## What are key considerations when paralleling power switches:

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<th>Effect on paralleling</th>
<th>Desired</th>
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<td>$R_{DS(on)}$</td>
<td>Affect static current sharing.</td>
<td>Positive temperature co-efficient for self-balancing</td>
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<td>Gate threshold, $V_{GS(th)}$</td>
<td>Impact dynamic current sharing during turn-on and off. Lower $V_{th}$ results in earlier turn-on and higher switching current/loss which creates positive feedback</td>
<td>Tight distribution, temperature independent or positive temperature co-efficient</td>
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<tr>
<td>Trans-conductance, $g_m$</td>
<td>Impact dynamic current sharing during turn-on and off.</td>
<td>Tight distribution, temperature independent or negative temperature co-efficient</td>
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<td>Circuit design and layout</td>
<td>Balanced circuit layout are important for dynamic current sharing and stability of the paralleling operation. <strong>This is particularly critical for high speed power switches such as GaN/SiC</strong></td>
<td>Minimize and equalize all layout parasitics to reduce circuit mismatch</td>
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<tr>
<td>Thermal</td>
<td>Affect the device temperature difference. $T_j$ variation may cause dynamic or static current sharing issues depending on device characteristics.</td>
<td>All paralleled devices should have similar thermal resistance and installed on same heatsink for good thermal balance.</td>
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- GaN E-HEMT has positive temperature co-efficient $R_{DS(on)}$
- Compared to SiC, strong temperature dependency of $R_{DS(on)}$ of GaN helps the current sharing in parallel operation
GaN E-HEMT has stable gate threshold over the temperature range

Si/SiC MOSFET $V_{GS(th)}$ decreases with temperature:
- Hotter drive turn-on earlier – *positive feedback*

SiC $V_{GS(th)}$ decreases with $T_J$

GaN E-HEMT $V_{GS(th)}$ is stable over $T_J$ range

No noticeable change from $T_J = 25$ to $150^\circ C$

-24% decrease
Trans-conductance, $g_m$ vs $T_J$

- GaN E-HEMT Trans-conductance $g_m$ decreases with temperature, good for paralleling
- This characteristics, together with stable $V_{GS(th)}$, helps with dynamic current sharing and self-balancing

**GaN HEMT**

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

$V_{GS(th)} = 50$

$I_D$ decreases at same $V_{GS}$ at higher $T_J$

$V_{GS(th)} = 25^\circ C$

$V_{GS(th)} = 150^\circ C$

**SiC MOSFET**

With same $V_{GS}$, $I_D$ increase at higher $T_J$

$V_{GS(th)}$

**SJ MOSFET**

Si: $V_{th}$ decreases and $g_m$ remain constant:
- Slightly positive feedback with $T_J$

**SiC:** $V_{GS(th)}$ drops and $g_m$ slightly increases:
- Hotter device tends to have higher switching current -> higher switching loss
- Positive feedback, potential thermal runaway if not designed properly

Figure 10: Typical $I_D$ vs. $V_{GS}$
Effect of $g_m$ on switching transient

- Negative feedback for self balancing in parallel:
  - $T_J \uparrow - g_m \downarrow - I_{D@switching} \downarrow - E_{on} \downarrow - T_J \downarrow$

2x GS66508T paralleled 400V/30A turn-on waveforms with different $T_J$

$I_{Q1} @ T_J = 25^\circ C$
- $E_{on} = 92 \mu J$

$I_{Q2} @ T_J = 125^\circ C$
- $E_{on} = 58 \mu J$
Circuit layout - Low inductance of GaNPX® package

GaNPX® package improves the paralleling performance and stability
- Traditional package has high source inductance that impacts paralleling performance
- GaNPX® package has ultra low Ls compared to traditional package
- Top-cooled T package features symmetric dual gate pads for easier layout

GaNPX® T Package
GS66516T (650V/25mΩ)

Ansys Q3D 3D modeling of GS66516T

TO-247 Package inductance

Package Source inductance
Ls=0.05nH

Ls = ~10-15nH
Circuit layout - advantages of GaN PX dual gate

- Dual gate reduces the total gate drive loop in paralleling design
- Easier to make symmetric gate drive layout
- Reduce total layout footprint area

2x TO-247 Parallel layout

2x GS66516T Parallel layout
Key design considerations for paralleling GaN

Compared to other technologies:

- GaN Systems E-HEMT characteristic is inherently good fit for paralleling as discussed.
  - The $R_{DS(on)}$ and GaN transfer characteristics provide strong negative feedback to self balance and compensate device and circuit mismatch

- Circuit layout is most critical to GaN: Ensure successful paralleling and optimum dynamic performance.

Therefore, this presentation will focus on gate drive and circuit layout discussion for dynamic performance of paralleling GaN:

- The impact of circuit parasitics on paralleling was analyzed
- A half bridge power stage with 4x paralleled GaN 650V/160A HEMTs was designed and validated by experimental test
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Key layout parasitics

Critical parasitic parameters that have high impact on GaN paralleling:

- **$L_{G1-4} \& L_{S1-4}$**: gate/source inductance
  - Unbalanced $L_G/L_S$ increases the gate ringing and risk of oscillation
    - Equalize $L_G/L_S$ using star connection and keep as low as possible
    - Individual $R_G/R_S$ is recommended to reduce gate ringing among paralleled devices

- **$L_{CS1-4}$**: Common source inductance
  - Defined as any inductance that couples power loop switching noise ($L\cdot\frac{di}{dt}$) into the gate drive circuit
  - Including the shared/common source inductance and mutual inductance between power and drive loops
  - Feedback switching $\frac{di}{dt}$ to $V_{GS}$, impact gate drive stability and performance
  - Minimize as much as possible.
Gate drive design for paralleled GaN

- For high current paralleling design, a small negative gate drive turn-off bias is recommended for lower turn-off loss and more robust gate drive. Recommend to use -3V to -5V with synchronous driving for optimum efficiency.
- Create bipolar gate drive from single power supply using a 6.2V Zener. Negative gate drive bias (VEE) is defined by PS1 output – Vzener(6V)
- Use small values (1-2Ω) for distributed gate and source resistance: R3/R5 and R6/R7
- Total turn-on $R_{G\_ON} = R_4 + R_3(R_5) + R_6(R_7)$. Turn off $R_{G\_OFF} = R_3(R_5) + R_6 (R_7)$
Flux cancelling for lower inductance

- When two adjacent conductors are located close with opposite current direction, magnetic flux generated by two current flows will cancel each other in the region highlighted.
- This magnetic flux canceling effect can lower the parasitic inductance.
- Arrange the layout so that high-frequency current flows in opposite direction on two adjacent PCB layers.
Flux Cancelling Design for half bridge layout

High Frequency Current alternates direction on Each Layer to provide flux canceling effect

Top Layer: place GaN HEMTs

Mid_L1: BUS+ -> Drain_High ; Source_Low -> BUS-
Mid_L2: Source_High -> Drain_Low
Mid_L3: BUS+ -> Drain_High ; Source_Low -> BUS-
Mid_L4: Source_High -> Drain_Low

Bottom Layer: place Gate Driver Circuit and Decoupling Caps
Comparison with Benchmark

GaN Systems Solution: only 25% $L_{\text{Loop}}$ of the Best Counterparts:

- Low inductance GaN$_{PX\text{®}}$ package
- Flux cancelling PCB design

Paralleling design considerations

Layout considerations for paralleling GaN

Design example of 4x paralleled GaN power stage

Experimental results
650V/240A high Power stage design using discrete GaN EHEMTs

- DC Bus Capacitor
- Low Side GaN E-HEMTs
- High Side GaN E-HEMTs
4x GS66516T Paralleling Test Board – Bottom View

- Low Side Gate Driver
- Decoupling Capacitors
- High Side Gate Driver
Layout of 4x paralleled GaN power stage

* Un-plated holes, for thermal measurement. Avoid routing electrical signals under the device.
Optimum Paralleling Layout for GaN HEMT (4x GS66516T)

Top side with 4x GS66516T in half bridge

- HV decoupling Cap
- Gate driver
- BUS+
- BUS-
- DC Link Cap

Bot side with gate driver

- Gate driver
- Gate driver
- Gate driver

Note symmetric gate drive layout:
- Utilize the dual gate on GS66516T GaNPx
- Gate resistor on each gate

Un-plated holes, for thermal measurement. Avoid routing electrical signals under the device.
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400V/240A double pulse hard Switching test waveforms

DUT: 4x GS66516T in parallel; Freewheeling: 4x GS66516T in parallel
Condition: \( V_{BUS} = 400V, I_{DS\_ON} = 231A, I_{DS\_OFF} = 240A, V_{GS} = +6.8V/-5V, R_{G\_ON} = 4.55\text{ohm}, R_{G\_OFF} = 1.25 \text{ ohm}. \)

- No-Derating Paralleling of GaN HEMTs. Hard switched up to full rated current with clean waveform.
- 400V/240A Hard Switching Capability with ~200V \( V_{DS} \) Margin

Experimental Waveform

- Measurement Setup: Lecroy WaveSurfer 10M Oscilloscope, HVD3106 Differential Probe(C1), CWT-3LFB mini Rogowski Coil(C2)

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Measure} & \text{P1: max(C1)} & \text{P2: max(C1)} & \text{P1: max(C2)} & \text{P2: max(C2)} \\
\hline
\text{value} & 450V & 440V & 450V & 440V \\
\hline
\text{status} & \checkmark & \checkmark & \checkmark & \checkmark \\
\hline
\end{array}
\]

\( \text{On: } dv/dt = 19.5V/\text{nS} \)
\( \text{Off: } dv/dt = 59.6V/\text{nS} \)
Summary

- Paralleling discrete GaN is desired to achieve higher power output
- GaN Systems E-HEMT device characteristics are inherently fit for paralleling:
  - Positive $R_{DS(ON)}$ temperature coefficient
  - Stable gate threshold over the temperature range
  - Negative tempco of $g_m$
  - Low inductance GaN $PX^\circledR$ package for minimum circuit mismatch

- Layout is critical for paralleling high speed GaN HEMT:
  - Low and balanced parasitic inductance on the power and gate drive loop. Equal length of gate drive layout and optimum gate driver circuit

- Summary
  - Provided practical design guide on how to parallel high speed GaN HEMT devices
  - Showed a design layout example of 4x paralleled GaN E-HEMT half bridge power stage
  - Hardware was built and GaN E-HEMT paralleled operation has been validated up to the rated current under hard switching test (400V/240A)