GS66508T/GS66516T-EVBDB GaN E-HEMT Daughter Board and GS665MB-EVB Evaluation Platform

User’s Guide

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DANGER!
This evaluation kit is designed for engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY. High voltage will be exposed on the board during the test and even brief contact during operation may result in severe injury or death.

Never leave the board operating unattended. After it is de-energized, always wait until all capacitors are discharged before touching the board.

CAUTION:
This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.
Overview

The GS665XXX-EVBDB daughter board style evaluation kit consists of two GaN Systems 650V GaN Enhancement-mode HEMTs (E-HEMTs) and all necessary circuits including half bridge gate drivers, isolated power supplies and optional heatsink to form a functional half bridge power stage. It allows users to easily evaluate the GaN E-HEMT performance in any half bridge-based topology, either with the universal mother board (P/N: GS665MB-EVB) or users’ own system design for quick prototyping.

Features:

- Serves as a reference design and evaluation tool as well as deployment-ready solution for easy in-system evaluation.
- Vertical mount style with height of 35mm, which fits in majority of 1U design and allows evaluation of GaN E-HEMT in traditional through-hole type power supply board.
- Current shunt position for switching characterization testing
- Universal form factor and footprint for all products

The daughter board and universal mother board ordering part numbers are below:

<table>
<thead>
<tr>
<th>Part Number</th>
<th>GaN E-HEMT P/N:</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS66502B-EVBDB</td>
<td>GS66502B</td>
<td>GaN E-HEMT 650V/7.5A, 200mΩ</td>
</tr>
<tr>
<td>GS66504B-EVBDB</td>
<td>GS66504B</td>
<td>GaN E-HEMT 650V/15A, 100mΩ</td>
</tr>
<tr>
<td>GS66508B-EVBDB</td>
<td>GS66508B</td>
<td>GaN E-HEMT 650V/30A, 50mΩ</td>
</tr>
<tr>
<td>GS66508T-EVBDB</td>
<td>GS66508T</td>
<td>GaN E-HEMT top side cooled 650V/30A, 50mΩ</td>
</tr>
<tr>
<td>GS66516T-EVBDB</td>
<td>GS66516T</td>
<td>GaN E-HEMT top side cooled 650V/60A, 25mΩ</td>
</tr>
<tr>
<td>GS665MB-EVB</td>
<td>GS665MB-EVB</td>
<td>Universal 650V Mother Board</td>
</tr>
</tbody>
</table>

Control and Power I/Os:

The daughter board GS665XXX-EVBDB circuit diagram is shown in Figure 1. The control logic inputs on 2x3 pin header J1 are listed below:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENA</td>
<td>Enable input. It is internally pulled up to VCC, a low logic disables all the PWM gate drive outputs.</td>
</tr>
<tr>
<td>VCC</td>
<td>+5V auxiliary power supply input for logic circuit and gate driver. On the daughter board there are 2 isolated 5V to 9V DC/DC power supplies for top and bottom switches.</td>
</tr>
<tr>
<td>VDRV</td>
<td>Optional 9V gate drive power input. This pin allows users to supply separate gate drive power supply. By default VDRV is connected to VCC on the daughter board via a 0 ohm jumper FB1. If bootstrap mode is used for high side gate drive, connect VDRV to 9V</td>
</tr>
<tr>
<td>PWMH</td>
<td>High side PWM logic input for top switch Q1. It is compatible with 3.3V and 5V</td>
</tr>
<tr>
<td>PWML</td>
<td>Low side PWM logic input for bottom switch Q2. It is compatible with 3.3V and 5V</td>
</tr>
<tr>
<td>0V</td>
<td>Logic inputs and gate drive power supply ground return.</td>
</tr>
</tbody>
</table>
The 3 power pins are:
- VDC+: Input DC Bus voltage
- VSW: Switching node output
- VDC-: Input DC bus voltage ground return. Note that control ground 0V is isolated from VDC-.

Figure 1 GS665XXX-EVBDB Evaluation Board Block Diagram

**GS66508T/GS66516T-EVBDB half bridge daughter board**

![Image of GS66508T/GS66516T-EVBDB bottom side](image)

Figure 2 GS66508T/GS66516T-EVBDB bottom side (without heatsink)
Figure 3 GS66508T/GS66516T-EVBDB top side

A. 2x GaN Systems 650V E-HEMT GS66508T(30A/50mΩ) or GS66516T (60A/25 mΩ). The PCB footprints are universal and compatible for both packages
B. 5V-9V isolated DC/DC gate drive power supply
C. Decoupling capacitors C4-C11
D. Isolated gate driver Silab Si8271
E. Optional current shunt position JP1.
F. Test points for bottom Q2 VGS.
G. Recommended probing positions for Q2 VDS.
H. Holes for temperature monitoring of Q1/Q2
I. M3 mounting screw for heatsink
J. (Optional) RC snubber circuit

GaN E-HEMTs:

- This daughter board includes two GaN Systems E-HEMT GS66508T (650V/30A, 50mΩ) or GS66516T (650V/60A, 25mΩ) in a GaNPx™ Top cooled T type package. The thermal pad on the top of device is internally connected to the source. Electrical insulation will be needed for heatsink attachment. GaNPx™ T package also features dual symmetrical gate for easier paralleling and PCB layout.

Figure 4 Package outline of GaNPx T Package
Gate drive power supply:

- Bipolar gate drive bias with +6V and -3V for turning off is chosen for this design for more robust gate drive and better noise immunity.
- 5V-9V isolated DC/DC converters are used for gate drive. 9V is then splitted into +6V and -3V bias by using 6V Zener diode
- By default gate drive supply input VDRV is tied to VCC +5V via 0Ω jumper (FB1). Remove FB1 if separate gate drive input voltage is to be used.

Gate driver circuit:

- Silab SI8271-GB-IS (3V UVLO) or SI8271-AB-IS (5V UVLO) isolated gate driver can be used for this design. Both drivers are compatible with 6V/-3V gate drive and has CMTI dv/dt immunity up to 200V/ns. It has separated source and sink drive outputs which eliminates the need for additional diode.
- GaN E-HEMT switching speed and slew rate can be directly controlled by the gate resistors. By default the turn-on Rgate (R6/R12) is 10Ω and Rg_off (R7/R14) is 2Ω. User can adjust the values of gate resistors to fine tune the turn-on and off speed.
- FB1/FB2 are footprints for optional ferrite bead. By default they are populated with 0Ω jumpers. If gate oscillation is observed, it is recommended to replace them with ferrite bead with Z=10-20Ω@100MHz.

![Gate bias and driver circuit](image)

Figure 5 Gate bias and driver circuit

RC Snubber:

RS1/CS1 and RS2/CS2 are place holders to allow user to experiment with RC snubber circuit (not installed). At high frequency operation the power dissipation for RS1/RS2 needs to be closely watched and CS1/CS2 should be sized correctly. It is recommended to start with 33-47pF and 10-20Ω.
Current shunt JP1:

- The board provides an optional current shunt position JP1 between the source of Q2 and power ground return. This allows drain current measurement for switching characterization test such as Eon/Eoff measurement.
- The JP1 footprint is compatible with T&M Research SDN series coaxial current shunt (recommended P/N: SDN-414-10, 2GHz B/W, 0.1Ω)
- If current shunt is not used JP1 must be shorted. JP1 affects the power loop inductance and its inductance should be kept as low as possible. Use a copper foil or jumper with low inductance.

![Diagram of current shunt](current-shunt-diagram.png)

Figure 6 Recommended probe connection with current shunt

**CAUTION:**
Check the JP1 before the first time use. To complete the circuit JP1 needs to be either shorted or a current shunt must be inserted before powering up.

Measurement with current shunt:

1. When measuring VSW with current shunt, ensure all channel probe grounds and current shunt BNC output case are all referenced to the source end of Q2 before the current shunt. The recommended setup of probes is shown as below.
2. The output of coaxial current shunt can be connected to oscilloscope via 50Ω termination impedance to reduce the ringing.
3. The measured current is inverted and can be scaled by using: \( I_d = \frac{V_{id}}{R_{sense}} \).
Thermal design:

1. GS66508T or GS66516T has a thermal pad at the top side for improved heat dissipation. Instead of relying on PCB for cooling, the heat can be transferred to heatsink directly from the top reducing the total thermal resistance.

2. A heatsink can be mounted to the board using a M3 screw with lock washer and nylon insulated bushing. Thermal Interface Material (TIM) is needed to provide electrical insulation and conformance to the thermal pad surface. The daughter board evaluation kit supplies with a 35x35mm heatsink with M3 tapped hole, and other heatsinks can also be used to fit users’ system design.

3. **Care should be taken during the assembly of heatsink to avoid PCB bending and mechanical stress to the GaN E-HEMT.** We recommend to limit the torque of M3 mounting screw to <1 in-lb (0.1Nm) for GS66508T and <2 in-lb (0.2Nm) for GS66516T, which translates to about ~50psi pressure on each device.

**WARNING!**

Over-torquing on the heatsink may create excess mechanical stress and could result in device failure. Always follow the maximum torque spec and attach the heatsink carefully to avoid any PCB bending or high pressing force on the devices.

4. To measure device case temperature, use IR camera or install thermocouple to monitor the temperature through two drilled holes from the top side as shown below:
CAUTION:
There is no on-board over-temperature protection. Device temperature must be closely monitored during the test. Never operate the board with device temperature exceeding $T_{J,\text{MAX}}$ (150°C).

5. The TIM we use on this assembly is Bergquist® SilPad 1500ST, the measured total thermal resistance can be found in Figure 9. Compared to bottom cooled design, T package eliminates the PCB thermal resistance and significantly improve the thermal performance. Thermal grease is typically not needed on the assembly. If thermal grease is to be applied, use non-conductive and non-capacitive type thermal grease.

6. Forced air cooling is recommended for power testing.
Figure 10 The daughter board assembly with heatsink attached
Using GS665XXX-EVBDB with universal mother board GS665MB-EVB

GaN Systems provides a universal 650V mother board (ordering part number: GS665MB-EVB, sold separately) that can be used as the basic evaluation platform for all the daughter boards.

The universal 650V mother board evaluation kit includes following items:

1. Mother board GS665MB-EVB
2. 12VDC Fan

12V input:

The board can be powered by 9-12V on J1. On-board voltage regulator creates to 5V for daughter board and control logic circuits. J3 is used for external 12VDC fan.

PWM control circuit:
The top and bottom switches PWM inputs can be individually controlled by two jumpers J4 and J6. Users can choose between a pair of complementary on-board internal PWM signals (non-inverted and inverted, controlled by J7 input) with dead time or external high/low side drive signals from J5 (users’ own control board).

An on-board dead time generation circuit is included on the mother board. Dead time is controlled by two RC delay circuits, R6/C12 and R5/C11. The default dead time is set to about 100ns. Additionally two potentiometers locations are provided (TR1/TR2, not included) to allow fine adjustment of the dead time if needed.
WARNING!
ALWAYS double check the jumper setting and PWM gate drive signals before applying power. Incorrect PWM inputs or jumper settings may cause device failures.

Test points:
Test points are designed in groups/pairs to facilitate probing:

<table>
<thead>
<tr>
<th>Test points</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP1/TP2</td>
<td>+5V/0V</td>
<td>5V bias power</td>
</tr>
<tr>
<td>TP7/TP8</td>
<td>PWMIN/0V</td>
<td>PWM input signal from J7</td>
</tr>
<tr>
<td>TP4/TP3/TP13</td>
<td>PWMH/PWML/0V</td>
<td>High/low side gate signals to daughter board</td>
</tr>
<tr>
<td>TP9/TP10</td>
<td>VDC+/VDC-</td>
<td>DC bus voltage</td>
</tr>
<tr>
<td>TP11/TP12</td>
<td>VOUT/VDC-</td>
<td>Output voltage</td>
</tr>
<tr>
<td>TP6/TP5</td>
<td>VSW/VDC-</td>
<td>Switching node output voltage (for HV oscilloscope probe)</td>
</tr>
</tbody>
</table>

Power connections:
CON1-CON7 mounting pads are designed to be compatible with following mounting terminals:
- #10-32 Screw mount,
- Banana Jack PCB mount (Keystone P/N: 575-4), or
- PC Mount Screw Terminal (Keystone P/N: 8191)

Output passives (L and C14)
An external power inductor (not included) can be connected between VSW (CON1) and VOUT (CON4/5) or VDC+ (CON2/3) for double pulse test. Users can choose their inductor size to meet the test requirement. Generally it is recommended to use power inductor with low inter-winding capacitance to obtain best switching performance. For the double pulse testing we use 2x 60uH/40Amp inductor (CWS, P/N: HF467-600M-40AV) in series. C14 is designed to accommodate a film capacitor as output filter.

Double pulse test mode
Double pulse test setup

Figure 14 Double pulse test setup

Double pulse test allows easy evaluation of device switching performance at high voltage/current without the need of actually running at high power. It can also be used for switching loss (Eon/Eoff) measurement and other switching characterization parameter test.

The circuit configuration and operating principle can be found in Figure 14:

1. The output inductor is connected to the VDC+.
2. At t0 when Q2 is switched on, the inductor current starts to ramp up until t1. The period of first pulse Ton1 defines the switching current $I_{SW} = \frac{V_{DS} \cdot T_{ON1}}{L}$.
3. t1-t2 is the free wheeling period when the inductor current $I_L$ forces Q1 to conduct in reverse.
4. t1 (turn-off) and t2 (turn-on) are of interest for this test as they are the hard switching transients for the half bridge circuit when Q2 is under high switching stress.
5. The second pulse t2-t3 is kept short to limit the peak inductor current at t3.

The double pulse signal can be generated using programmable signal generator or microcontroller/DSP board. As this test involves high switching stress and high current, it is recommended to set the double pulse test gate signal as single trigger mode or use long repetition period (for example >50-100ms) to void excess stress to the switches. Q1 can be kept off during the test or driven synchronously (J4 set to OFF or INT_INV) and Q2 is set to INT (or EXT position if PWM signal is from J5).

**WARNING!**

Limit the maximum switching test current to 30A for GS66508T (60A for GS66516T) and ensure maximum drain voltage including ringing is below 650V for pulse testing. Exceeding this limit may cause damage to the devices.
Buck/Standard half bridge mode

This is standard half bridge configuration that can be used in following circuits:
- Synchronous Buck DC/DC
- Single phase half bridge inverter
- ZVS half bridge LLC
- Phase leg for full bridge DC/DC or
- Phase leg for a 3-phase motor drive

Jumper setting:
- J4 (Q1): INT
- J6 (Q2): INT_INV

Boost mode

When the output becomes the input and the load is attached between VDC+ and VDC-, the board is converted into a boost mode circuit and can be used for:
- Synchronous Boost DC/DC
- Totem pole bridgeless PFC

Jumper setting:
- J4 (Q1): INT_INV
- J6 (Q2): INT
Using GS665XXX-EVBDB in system:

The daughter board allows users to easily evaluate the GaN performance in their own systems. Refer to the footprint drawing of GS665XXX-EVBDB as shown below:

1. All units are in mm.
2. Pin 1-6: Dia. 1mm

Figure 15 Recommended footprint drawing of daughter board GS665XXX-EVBDB
Quick Start procedure – Double pulse test

Follow the instructions below to quickly get started with your evaluation of GaN E-HEMT. Equipment and components you will need:

- Four-channel oscilloscope with 500MHz bandwidth or higher
- High bandwidth (500MHz or higher) passive probe
- High bandwidth (500MHz) high voltage probe (>600V)
- AC/DC current probe for inductor current measurement
- 12V DC power supply
- Signal generator capable of creating testing pulses
- High voltage power supply (0-400VDC) with current limit.
- External power inductor (recommend toroid inductor 50-200uH)

1. Check the JP1 on daughter board GS665XXX-EVBDB. Use a copper foil and solder to short JP1.
2. Install GS665XXX-EVBDB on the mother board. Press all the way down until you feel a click. Connect probe between VGL and VSL for gate voltage measurement.
3. Set up the mother board:
   a. Connect 12VDC bias supply to J1.
   b. Connect PWM input gate signal (0-5V) to J7. If it is generated from a signal generator ensure the output mode is high-Z mode.
   c. Set J4 to OFF position and J7 to INT.
   d. Set High voltage (HV) DC supply voltage to 0V and ensure the output is OFF. Connect HV supply to CON2 and CON6.
   e. Use HV probe between TP6 and TP5 for Vds measurement.
   f. Connect external inductor between CON1 and CON3. Use current probe to measure inductor current IL.
4. Set up and check PWM gate signal:
   a. Turn-on 12VDC power.
   b. Check the 2 LEDs on the daughter board. They should be turned on indicating the isolated 9V is present.
   c. Set up signal generator to create the waveforms as shown in Figure 14. Use equation Isw = (VDS*TON1) / L to calculate the pulse width of the first pulse and ensure the Isw_max is ≤30A at 400VDC.
   d. Set the operation mode to either single trigger or Burst mode with repetition period of 100ms.
   e. Turn on the PWM output and check on the oscilloscope to make sure the VGL waveform is present and matches the PWM input.
5. Power-on:
   a. Turn on the output of the HV supply. Start with low voltage and slowly ramp the voltage up until it reaches 400VDC. During the ramping period closely observe the voltage and current waveforms on the oscilloscope.
6. Power-off:
   a. After the test is complete, slowly ramp down the HV supply voltage to 0V and turn off the output. Then turn off the 12V bias supply and signal generator output.
Figure 16 Double pulse test setup example
Test results

Double Pulse test ($V_{DS}=400V$, $I_{MAX}=30A$, $L=120uH$, $R_{G(ON)}=10\Omega$, $R_{G(OFF)}=2\Omega$, $V_{GS}=+6/-3V$):

![Figure 17 400V/30A double pulse test waveform (GS66508T)](image)

Figure 17 shows the hard switching on waveforms at 400V/30A. A Vds dip can be seen due to the rising drain current ($di/dt$ in the power loop $\Delta V=Lp\times di/dt$, where $Lp$ is the total power loop inductance). After the drain current reaches the inductor current, the Vds starts to fall. The Vgs undershoot spike is caused by the miller feedback via Cgd under negative $dv/dt$.

Due to the low gate charge and small $R_{G(OFF)}$, GaN E-HEMT gate has limited control on the turn-off $dv/dt$. Instead the Vds rise time is determined by how fast the turn-off current charges switching node capacitance (Coss).

The low Coss of GaN E-HEMT and low parasitic inductance of GaNPX™ package together with optimized PCB layout, enables a fast and clean turn-off Vds waveform with only 50V the turn-off Vds overshoot at $dv/dt > 100V/ns$. The measured rise time is 3.9ns at 400V and 30A hard turn-off.
a) hard switching turn-on 400V/30A  

b) hard switching turn-off 400V/30A  

Figure 18 Double puls test switching transient waveforms (GS66508T)  

Switching Loss energy (Eon/Eoff) measurement  

A T&M search coaxial current shunt (SDN-414-10, 0.1Ω) is installed for switching loss measurement as shown below.  

Figure 19 Eon/Eoff measurement probe connection with current shunt
The switching energy can be calculated from the measured switching waveform $P_{sw} = V_{ds} \cdot I_{d}$. The integral of the $P_{sw}$ during switching period is the measured switching loss. The channel deskewing is critical for measurement accuracy. It is recommended to manually deskew $I_{d}$ against $V_{ds}$ as shown in Figure 21. The drain current spike is caused by charging the high side switch $Coss$ ($Qoss$ loss).

Figure 20 Eon/Eoff measurement and test bench setup

Figure 21 Turn-on switching loss measurement ($E_{on}=87\mu J$, 400V/30A, $T_{J}=25^\circ C$)
Figure 22 Turn-off switching loss measurement (Eoff=15μJ, 400V/30A, TJ=25°C)

The switching loss measurements with drain current from 0 to 30A for GS66508T or up to 60A for GS66516T can be found in Figure 23. The turn-on loss dominates the overall hard switching loss. Eon at 0A is the Qoss loss caused by the Coss at high side switch.

Figure 23 GS66508T Switching Loss Measurement (VDS = 400V, TJ=25°C)
Synchronous Buck Test (L=120uH, VIN=400V, VOUT=200V, D=50%, FSW=100 kHz, POUT =0-2.4kW)

The board is converted to a synchronous buck DC/DC converter and demonstrates efficiency close to 99% at 2kW. With forced air cooling, the board is tested up to 2kW for GS66508T with device temperature Tjmax = 75 °C and 2.4kW for GS66516T with Tjmax <70°C.
Figure 25 Synchronous Buck Efficiency and thermal measurement

Figure 26 Thermal image (GS66516T, Pout=2.4kW)
Appendix A - GS66508T/GS66516T-EVBDB

Circuit schematics-GS66508T EVBDB
PCB layout

Top Layer

Mid Layer 1

Mid Layer 2

Bottom Layer
# Bill of Materials

<table>
<thead>
<tr>
<th>Q</th>
<th>Reference</th>
<th>Description</th>
<th>Value</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCB</td>
<td>PCB bare 4-layer 2oz Cu.</td>
<td>● ●</td>
<td>generic</td>
<td>generic</td>
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<tr>
<td>3</td>
<td>CON1, CON2, CON3</td>
<td>CONN PC PIN EDGE MNT</td>
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<td>CAP, CER, 4.7UF, 25V, +/-10%, X7R, 0805</td>
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<td>TAIYO YUDEN</td>
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<td>GS66508T</td>
<td>GaN Systems</td>
<td>GS66508T</td>
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<tr>
<td>2</td>
<td>Q1B, Q2B</td>
<td>GaN E-HEMT 650V/60A TOP COOL</td>
<td>GS66516T</td>
<td>GaN Systems</td>
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<td>R5, R6, R11, R12</td>
<td>RES, 10R, 1%, 1/10W, 0603</td>
<td>10R</td>
<td>generic</td>
<td>generic</td>
</tr>
<tr>
<td>2</td>
<td>R7, R14</td>
<td>RES, 2R, 1%, 1/10W, 0603</td>
<td>2R</td>
<td>generic</td>
<td>generic</td>
</tr>
<tr>
<td>2</td>
<td>R15, R16</td>
<td>RES, 1K, 1%, 1/10W, 0603</td>
<td>1K0</td>
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<td>generic</td>
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<tr>
<td>6</td>
<td>TP1, TP2, TP3, TP4, TP5, TP6</td>
<td>Probe test point</td>
<td>CON-TP-1POS</td>
<td>DO NOT INSTALL</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>TP7, TP8, TP9, TP10</td>
<td>Probe test point</td>
<td>CON-TP-1POS</td>
<td>DO NOT INSTALL</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>U2, U4</td>
<td>IC ISO GATE DRIVER 2.5KV HIGH CMTI</td>
<td>SI8271GB-IS</td>
<td>SILICON LABS</td>
<td>SI8271GB-IS</td>
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</tbody>
</table>

**Assembly Notes:**
- Marking positions 02/15-15-542-1014 (on board)
- For bootstrap mode, DO NOT INSTALL.
- Use wide copper foil to short the connection if not used.
- For current measurement, footprint compatible with T&M SDN-414-010 current shunt. Use wide copper foil to short the connection if not used.
- For bootstrap mode, DO NOT INSTALL.

**Parts:**
- Heatsink, 35x35mmx25.4mm, customized
- Electrically insulated Thermal pad
- M3  screw w/ insulated sleeve

**Note:**
Please refer to the Evaluation Board/Kit Important Notice on page 32.
Appendix B - GS665MB-EVB

Circuit schematics
Assembly drawing

**Assembly Top**

TOP COMPONENT SIDE

SUGGESTED LOCATION FOR S/N LABEL

**Assembly Bottom**
# Bill of Materials

<table>
<thead>
<tr>
<th>Reference</th>
<th>Part number</th>
<th>Description</th>
<th>Value</th>
<th>Manufacturer</th>
<th>Manufacturer Code</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>PCB</td>
<td>PCB bare 2-layer 2oz Cu.</td>
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<td></td>
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<tr>
<td>2</td>
<td>CON1, CON2, CON3, CON4, CON5, CON6, CON7</td>
<td>TERMINAL SCREW VERTICAL PC MNT</td>
<td>CON-10-32-SCRWMNT</td>
<td>KEYSTONE</td>
<td>8191</td>
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<tr>
<td>3</td>
<td>CON8, CON9, CON10</td>
<td>TERMINAL SCREW VERTICAL PC MNT</td>
<td>CON-10-32-SCRWMNT</td>
<td>KEYSTONE</td>
<td>8191</td>
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<tr>
<td>4</td>
<td>C1</td>
<td>CAP ALUM 220UF 20% 25V SMD</td>
<td>220uF 25V</td>
<td>Panasonic</td>
<td>EEE-FK1E221P</td>
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<tr>
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<td>C2, C3, C4</td>
<td>GENERIC 1UF/25V, 10% X7R SMD 0603</td>
<td>1uF</td>
<td>TAIYO YUDEN</td>
<td>TMK107B7105KA-T</td>
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<tr>
<td>6</td>
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<td>GENERIC 10UF/25V, 10% SMD 0805</td>
<td>10uF</td>
<td>TAIYO YUDEN</td>
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<tr>
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<td>C9</td>
<td>GENERIC 0.1UF/25V, 10% X7R SMD 0603</td>
<td>0.1uF</td>
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<td>TMJ107BB7104KAHT</td>
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<tr>
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<td>0.1uF</td>
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<td>TMJ107BB7104KAHT</td>
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<tr>
<td>9</td>
<td>C13, C14</td>
<td>CAP FILM 10UF/600VDC 5%, 27.5MM LEAD SPACING</td>
<td>10uF 700V</td>
<td>KEMET</td>
<td>C4AEHBU5100A11J</td>
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<tr>
<td>10</td>
<td>D1, D2</td>
<td>DIODE SCHOTTKY 20V 500MA SOD523</td>
<td>PMEG2005EB</td>
<td>NXP</td>
<td>03120153427100</td>
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<td>11</td>
<td>J1</td>
<td>TERM BLOCK HDR 2POS R/A 5.08MM</td>
<td>CON-TERM-BLK-2POS-RA</td>
<td>TE CONNECTIVITY</td>
<td>796638-2</td>
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<tr>
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<td>J1-PLUG</td>
<td>TERM BLOCK BLUG 2POS 5.08MM</td>
<td>TE CONNECTIVITY</td>
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<tr>
<td>13</td>
<td>J2</td>
<td>CONN RCPT 6POS .100 DBL STR PCB</td>
<td>CON-RCPT-2X3-BOT</td>
<td>HARWIN</td>
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<td>14</td>
<td>J3</td>
<td>CONNECTOR FOR 12V FAN, DO NOT INSTALL</td>
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<td>CON-JMP-4POS</td>
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<td>CONN 8-POS, DUAL ROW 2.54MM</td>
<td>CON-HDR-4X2</td>
<td>AMPHENOL</td>
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<td>17</td>
<td>J7</td>
<td>CONN BNC JACK STR 50 OHM PCB</td>
<td>112538</td>
<td>AMPHENOL</td>
<td>112538</td>
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<td>18</td>
<td>J8, J9, J10</td>
<td>CONN RECEPT PIN .032-.046&quot; .075&quot;</td>
<td>CON-RCPT-EDGEMNT</td>
<td>MILLMAX</td>
<td>MATE-MAX-00000000000</td>
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<td>19</td>
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<td>VISHAY DALE</td>
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<td>TEST POINT PCB</td>
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<td>TR1, TR2</td>
<td>2K</td>
<td>RECOM</td>
<td>CMC-08</td>
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<td>T1</td>
<td>COMM MODE CHOKE 5.2A T/H</td>
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<tr>
<td>25</td>
<td>U1</td>
<td>IC REG LDO 5V 1A DPAK</td>
<td>MC7805BDTRKG</td>
<td>ON SEMI</td>
<td>MC7805</td>
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<tr>
<td>26</td>
<td>U2</td>
<td>IC GATE NAND 4CH 2-INP 14-SOIC</td>
<td>74VHC132</td>
<td>FAIRCHILD</td>
<td>74VHC132</td>
</tr>
</tbody>
</table>

Off the board components:
- M1, M2, M3, M4, M5, M6: PCB STANDOFF NYLON STACKABLE 4.75MM HOLE MECH-STDOFF-KEYSTONE-8830 KEYSTONE 8833
- FAN: FAN AXIAL 38X20MM 12VDC WIRE SUNON FANS PMD1238PKB1-A.(2).GN
- JUMPER JUMPER SHUNT GENERIC TE CONNECTIVITY M20-3185422 |

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