Parasitic Capacitance $E_{qoss}$ Loss Mechanism, Calculation, and Measurement in Hard-Switching for GaN HEMTs

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1. Introduction
2. $E_{qoss}$ loss mechanism
3. $E_{qoss}$ loss calculation
4. $E_{qoss}$ loss measurement method and experimental verification
5. Conclusions
1. Introduction

- GaN HEMTs can be applied to both soft-switching and hard-switching applications.
- For soft-switching ZVS technique, the turn-on switching loss is zero.
- This application note is about the parasitic capacitance loss during the turn-on of the hard-switching application.
Hard-switching transition of Si MOSFET

1. Snappy reverse recovery
2. High \( E_{\text{on}} \) loss
3. High \( \frac{dI}{dt} \), parasitic ringing

**Math:** \( V_{\text{DS}} \times I_D \)

Si MOSFET \( E_{\text{on}} = 6670 \mu \text{J} \)

Hard switching turn-on of a Si SJ MOSFET @ 400V/22A
2. $E_{qoss}$ loss mechanism

Hard-switching transition of GaN E-HEMT

1. Much lower turn-on loss
2. No snappy recovery and uncontrolled high $dl_r/dt$
3. Clean waveforms

Hard switching turn-on of a GaN E-HEMT @ 400V/22A

- Zero $Q_{rr}$ loss
- Zero $Q_{rr}$ period

Switch commutation operating principle of GaN HEMT
2. $E_{qoss}$ loss mechanism

Hard-switching loss distribution

Hard switching turn-on of a Si SJ MOSFET @ 400V/22A

Math: $V_{DS} \cdot I_D$

Hard switching turn-on of a GaN E-HEMT @ 400V/22A

Math: $V_{DS} \cdot I_D$

Hard-switching turn-on loss of Si MOSFET

Hard-switching turn-on loss of GaN HEMT
### 2. $E_{qoss}$ loss mechanism

#### Switching loss distribution of GaN HEMT

<table>
<thead>
<tr>
<th>Loss distribution</th>
<th>External measurement</th>
<th>Intrinsic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-on loss $E_{on}$</td>
<td>$E_{Vlion} + E_{qoss}$</td>
<td>$E_{Vlion} + E_{qoss} + E_{oss}$</td>
</tr>
<tr>
<td>Turn-off loss $E_{off}$</td>
<td>$E_{Vloff} + E_{oss}$</td>
<td>$E_{Vloff}$</td>
</tr>
</tbody>
</table>

- $E_{qoss}$ and $E_{oss}$ loss affect the overall $E_{on}$ loss, especially under light load operating condition.
- Accurate $E_{qoss}$ and $E_{oss}$ loss calculations are necessary.

**External measured $E_{on}/E_{off}$ switching loss distribution**

**Intrinsic $E_{on}/E_{off}$ switching loss distribution**


3. $E_{qoss}$ loss calculation

- $E_{oss}$ loss calculation equation does not apply to $E_{qoss}$.

$$E_{oss} \text{ loss: } E_{oss} = \int_0^{V_{dc}} V_{ds} \cdot C_{oss}(V_{ds}) dV_{ds}$$

- $E_{qoss}$ loss is higher than $E_{oss}$ loss, as usually the $C_{oss}$ of the device is higher at lower voltage $V_{ds}$ region.

$$E_{qoss} \text{ loss: } E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) \cdot C_{oss}(V_{ds}) dV_{ds}$$

Parasitic capacitance $C_{oss}$

$E_{oss}/E_{qoss}$ loss of GS66508T at different operating voltage
$E_{\text{qoss}}$ loss comparison with Si MOSFET

- The capacitance $C_{\text{oss}}$ of Si MOSFET is more nonlinear than GaN's.
- Much higher $C_{\text{oss}}$ value under low voltage region.
- $E_{\text{qoss}}$ loss of Si MOSFET is significantly larger.

\[ \Delta C = 120 \times \]

Comparison of parasitic capacitance $C_{\text{oss}}$

Comparison of $E_{\text{qoss}}$ loss under 400V

Comparison of $E_{\text{qoss}}$ loss under different $V_{ds}$
On double pulse test (DPT) circuit, the measured $E_{\text{oss}}/E_{\text{qoss}}$ also includes the parasitic capacitances from PCB and inductor. Taking $C_{\text{pcb}}$ and $C_{\text{pl}}$ into account:

$$E_{\text{oss}} = \int_0^{V_{\text{dc}}} V_{\text{ds}} \cdot C_{\text{oss}(V_{\text{ds}})} dV_{\text{ds}} + \frac{1}{2} (C_{\text{pl}} + C_{\text{pcb}}) V_{\text{dc}}^2$$

$$E_{\text{qoss}} = \int_0^{V_{\text{dc}}} (V_{\text{dc}} - V_{\text{ds}}) \cdot C_{\text{oss}(V_{\text{ds}})} dV_{\text{ds}} + \frac{1}{2} (C_{\text{pl}} + C_{\text{pcb}}) V_{\text{dc}}^2$$

- A Q3D simulation has been performed on the GS66508T evaluation board.
- The total voltage-independent capacitance is about 20 pF.
A. Load current independence

- Several double pulse tests based on GS66516T under different load currents were performed.
- The load current independence of the current bump also indicates the absence of body diode.
B. $E_{qoss}$ loss measurement method

- During the DPT, the $E_{qoss}$ can be measured either upon turn-on of the first pulse or on the turn-on of the second pulse.

- In order to simplify the $E_{qoss}$ loss measurement, the loss is measured at the turn-on of the first pulse which the V/I loss is zero.
C. \( E_{qoss} \) loss measurement setup

- To verify the impact factor and also the value of the loss, the DPT platform with closed-loop temperature control is applied.
D. Junction temperature and switching speed independence

• \( R_{g\_on} \) is chosen as 30 ohm and 50 ohm, as the purpose of the test is to prove the switching speed independence and also measure the \( E_{qoss} \) energy loss as accurate as possible.

- 100 Vdc with \( T_j=75^\circ C \) and \( R_{g\_on}=30 \) ohm
- 200 Vdc with \( T_j=25^\circ C \) and \( R_{g\_on}=30 \) ohm
- 300 Vdc with \( T_j=25^\circ C \) and \( R_{g\_on}=50 \) ohm
- 400 Vdc with \( T_j=75^\circ C \) and \( R_{g\_on}=30 \) ohm
Summary on $E_{qoss}$ loss measurement

- Test results are consistent which indicates $E_{qoss}$ is also independent on the junction temperature and switching speed.

- By considering the other parasitic capacitances, the discrepancy between the theoretical values and measured values is relatively small, verifying the calculation method.

![Graph showing measured results with different $T_j$ and $R_g$](image1)

![Graph comparing measurement and calculation results](image2)
5. Conclusions

- Detailed $E_{qoss}$ loss mechanism, calculation and measurement method for GaN HEMTs are presented.

- The $E_{qoss}$ loss of GaN HEMT is significantly lower compared with Si MOSFET.

- Experimental results verify the $E_{qoss}$ loss calculation method and also prove that the loss is only a function of voltage and the corresponding capacitances.

- The accurate $E_{qoss}$ loss calculation yields a more accurate $E_{on}$ loss estimation, especially under light load condition.