Design considerations of Paralleled GaN HEMT-based Half Bridge Power Stage

Last update: March 12, 2018

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- ❑ Layout considerations for paralleling GaN
- ❑ Design example of 4x paralleled GaN power stage
- ❑ Experimental results

Paralleling design considerations

GaN Systems

What are key considerations when paralleling power switches:

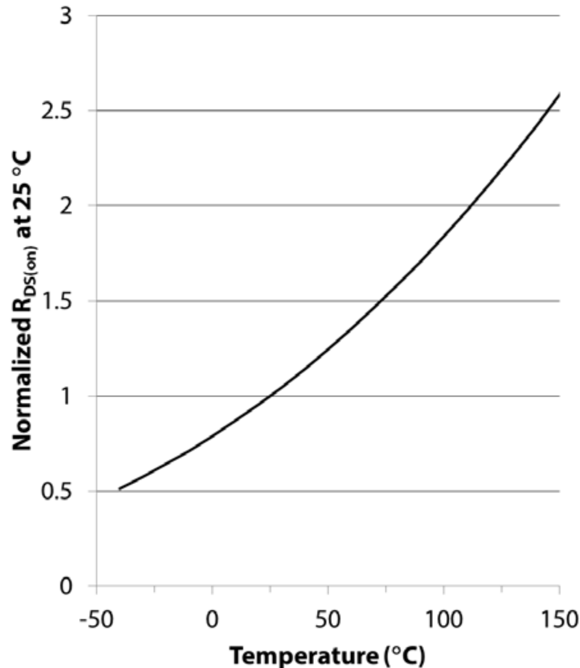
Design parameters	Effect on paralleling	Desired
$R_{DS(on)}$	Affect static current sharing.	Positive temperature co-efficient for self-balancing
Gate threshold, $V_{GS(th)}$	Impact dynamic current sharing during turn-on and off. Lower Vth results in earlier turn-on and higher switching current/loss which creates positive feedback	Tight distribution, temperature independent or positive temperature co-efficient
Trans-conductance, g_m	Impact dynamic current sharing during turn-on and off.	Tight distribution, temperature independent or negative temperature co-efficient
Circuit design and layout	Balanced circuit layout are important for dynamic current sharing and stability of the paralleling operation. **This is particularly critical for high speed power switches such as GaN/SiC**	Minimize and equalize all layout parasitics to reduce circuit mismatch
Thermal	Affect the device temperature difference. Tj variation may cause dynamic or static current sharing issues depending on device characteristics.	All paralleled devices should have similar thermal resistance and installed on same heatsink for good thermal balance.

$R_{DS(on)}$ vs T_J

GaN Systems

- GaN E-HEMT has positive temperature co-efficient $R_{DS(on)}$
- Compared to SiC, strong temperature dependency of $R_{DS(on)}$ of GaN helps the current sharing in parallel operation

GaN E-HEMT $R_{DS(on)}$ vs T_J



SiC $R_{DS(on)}$ vs T_J

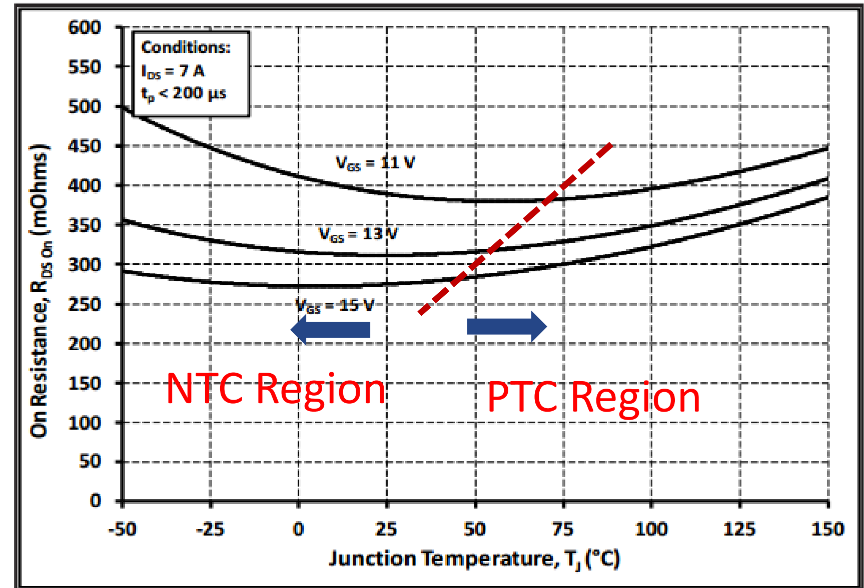
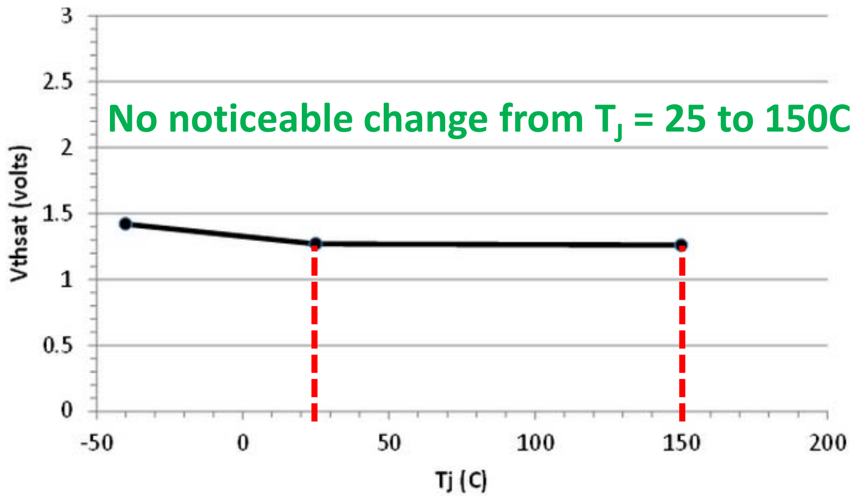


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

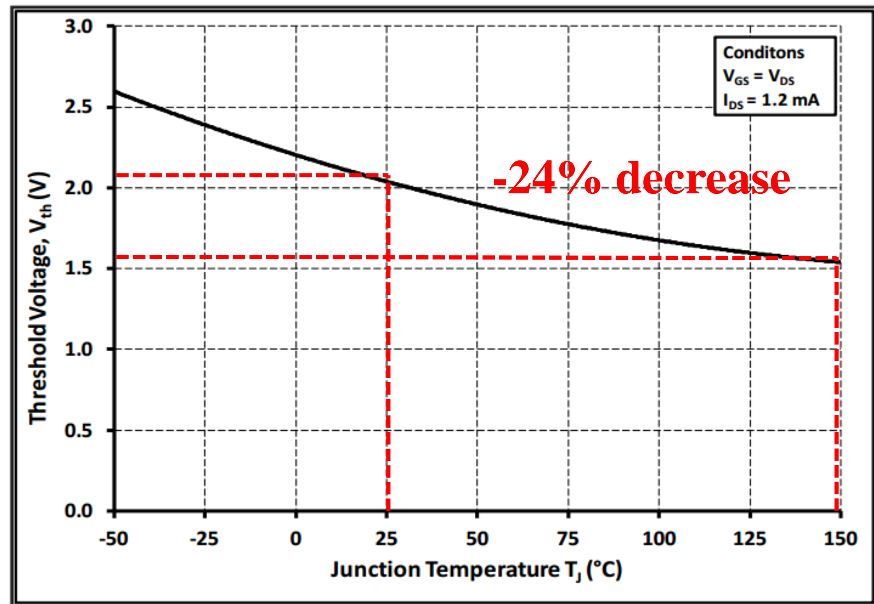
$V_{GS(th)}$ vs T_J

- GaN E-HEMT has stable gate threshold over the temperature range
- Si/SiC MOSFET $V_{GS(th)}$ decreases with temperature:
  - *Hotter drive turn-on earlier – positive feedback*

GaN E-HEMT $V_{GS(th)}$ is stable over T_J range



SiC $V_{GS(th)}$ decreases with T_J



Trans-conductance, g_m vs T_J

GaN Systems

- GaN E-HEMT Trans-conductance g_m decreases with temperature, good for paralleling
- This characteristics, together with stable $V_{GS(th)}$, helps with dynamic current sharing and self-balancing

GaN HEMT

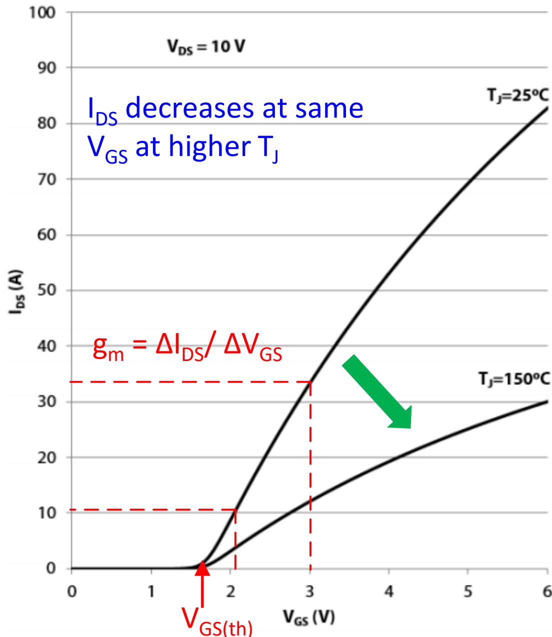
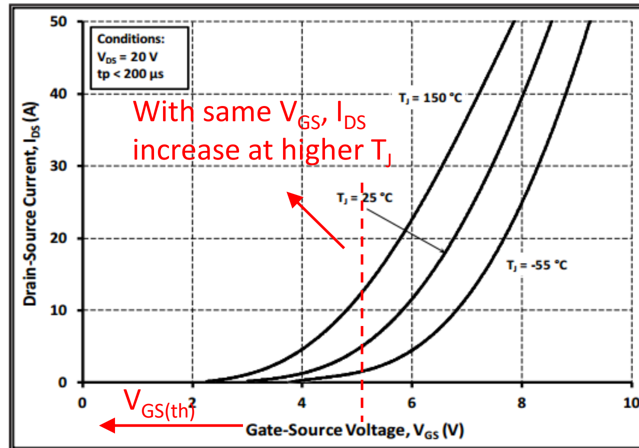


Figure 10 : Typical I_{DS} vs. V_{GS}

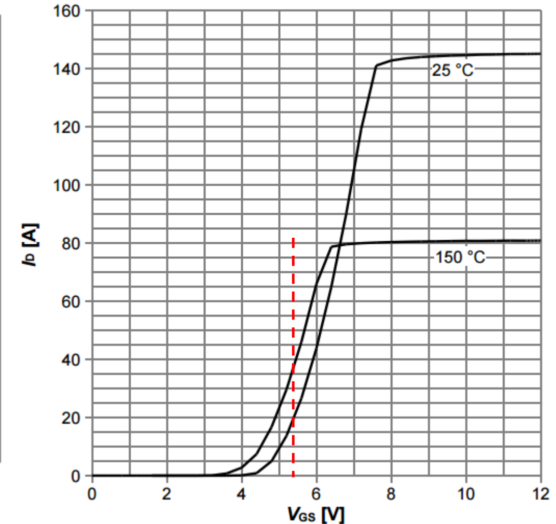
SiC MOSFET



SiC: $V_{GS(th)}$ drops and gm slightly increases:

- ***Hotter device tends to have higher switching current -> higher switching loss***
- ***Positive feedback, potential thermal runaway if not designed properly***

SJ MOSFET



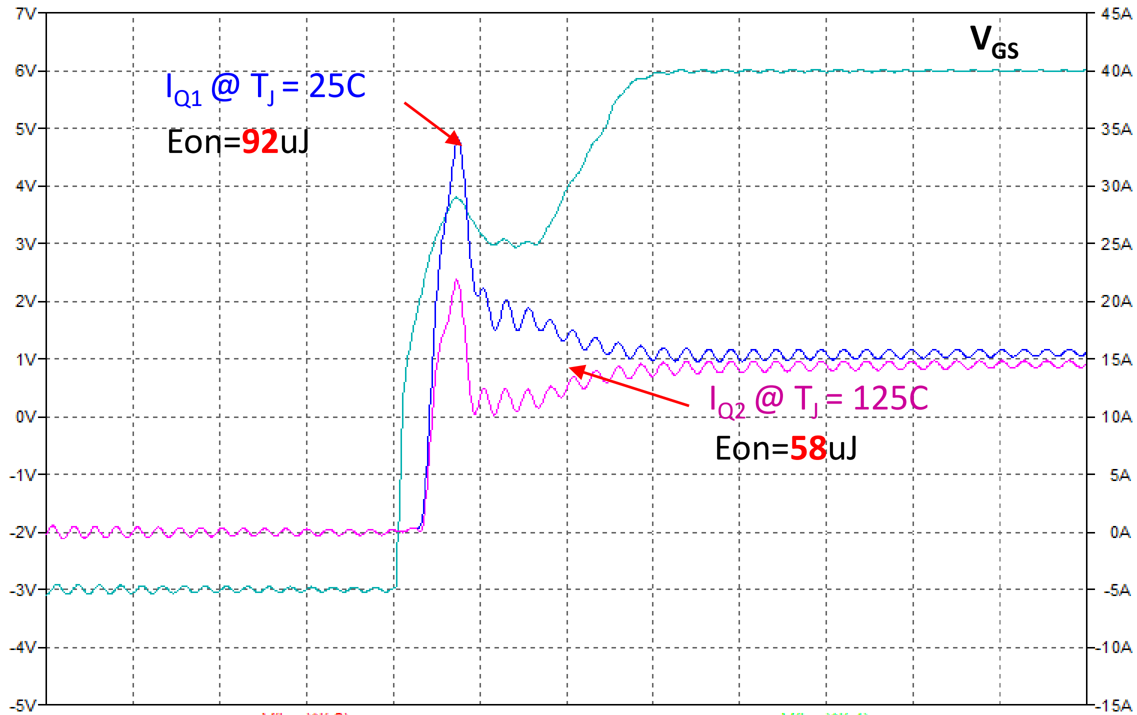
Si: Vth decreases and gm remain constant:

- ***Slightly positive feedback with T_J***

Effect of g_m on switching transient

- Negative feedback for self balancing in parallel:
- T_J ↗ - g_m ↘ - $I_{D@switching}$ ↘ - E_{on} ↘ - T_J ↘

2x GS66508T paralleled 400V/30A turn-on waveforms with different T_J

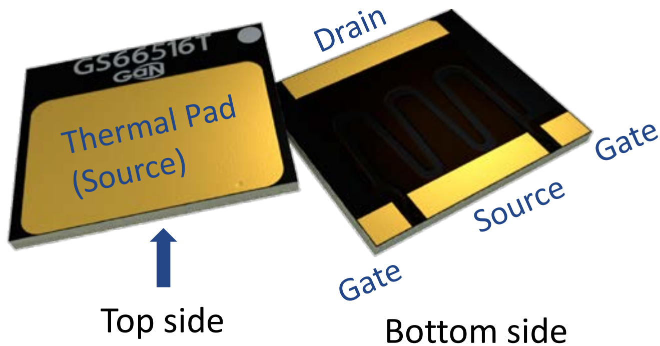


Circuit layout - Low inductance of GaN*PX*® package

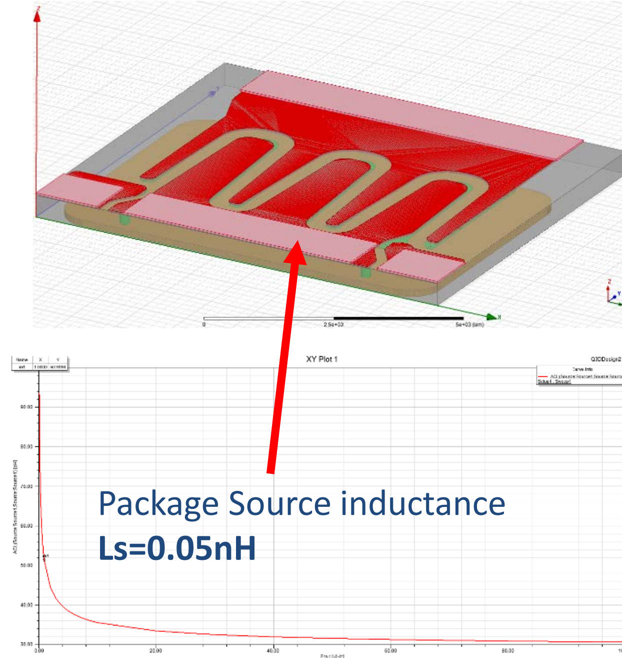
GaN*PX*® package improves the paralleling performance and stability

- Traditional package has high source inductance that impacts paralleling performance
- GaN*PX*® package has ultra low Ls compared to traditional package
- Top-cooled T package features symmetric dual gate pads for easier layout

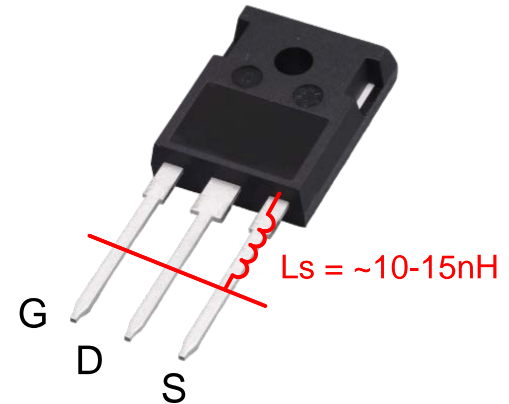
GaN*PX*® T Package
GS66516T (650V/25mΩ)



Ansys Q3D 3D modeling of GS66516T



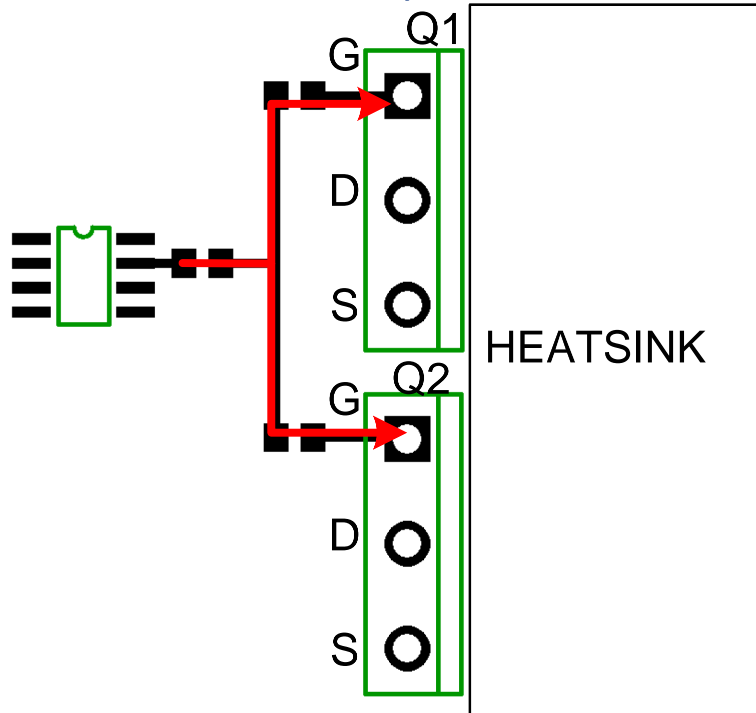
TO-247 Package inductance



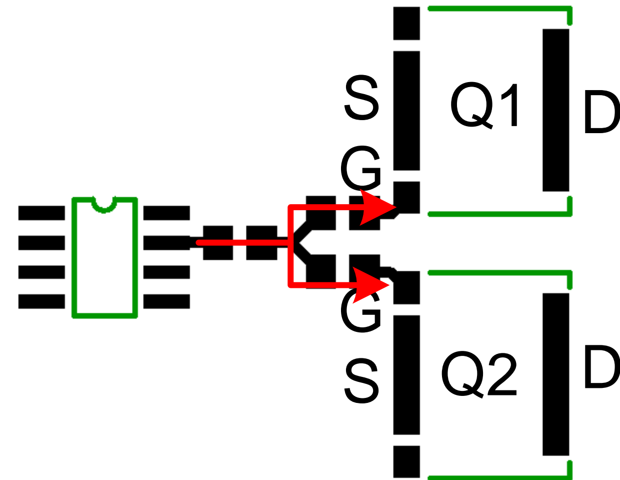
Circuit layout - advantages of GaN*PX* dual gate

- Dual gate reduces the total gate drive loop in paralleling design
- Easier to make symmetric gate drive layout
- Reduce total layout footprint area

2x TO-247 Parallel layout



2x GS66516T Parallel layout



Key design considerations for paralleling GaN

GaN Systems

Compared to other technologies:

- GaN Systems E-HEMT characteristic is inherently good fit for paralleling as discussed.
  - The $R_{DS(on)}$ and GaN transfer characteristics provide strong negative feedback to self balance and compensate device and circuit mismatch
- ***Circuit layout is most critical to GaN: Ensure successful paralleling and optimum dynamic performance.***
- Therefore, this presentation will focus on gate drive and circuit layout discussion for dynamic performance of paralleling GaN:
  - The impact of circuit parasitics on paralleling was analyzed
  - A half bridge power stage with 4x paralleled GaN 650V/160A HEMTs was designed and validated by experimental test

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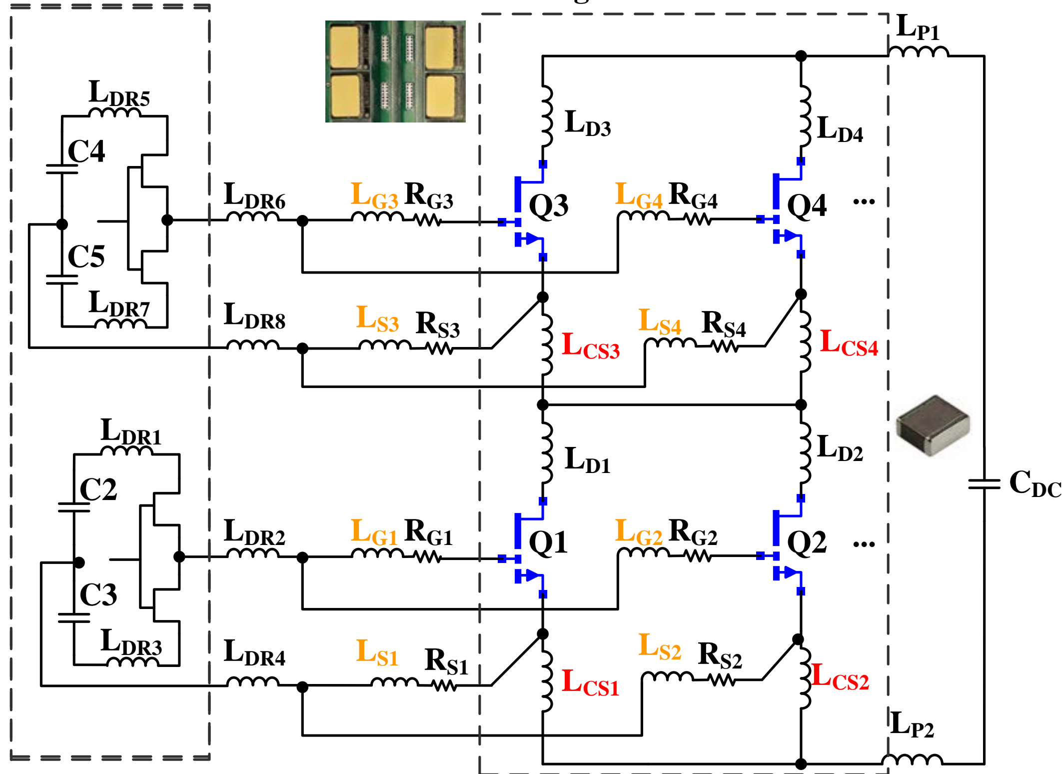
Key layout parasitics

GaN Systems



Critical parasitic parameters that have high impact on GaN paralleling:

$L_{G1\text{-}4}$ & $L_{S1\text{-}4}$: gate/source inductance

Unbalanced L_G/L_S increases the gate ringing and risk of oscillation

- Equalize L_G/L_S using star connection and keep as low as possible
- **Individual R_G/R_S is recommended to reduce gate ringing among paralleled devices**

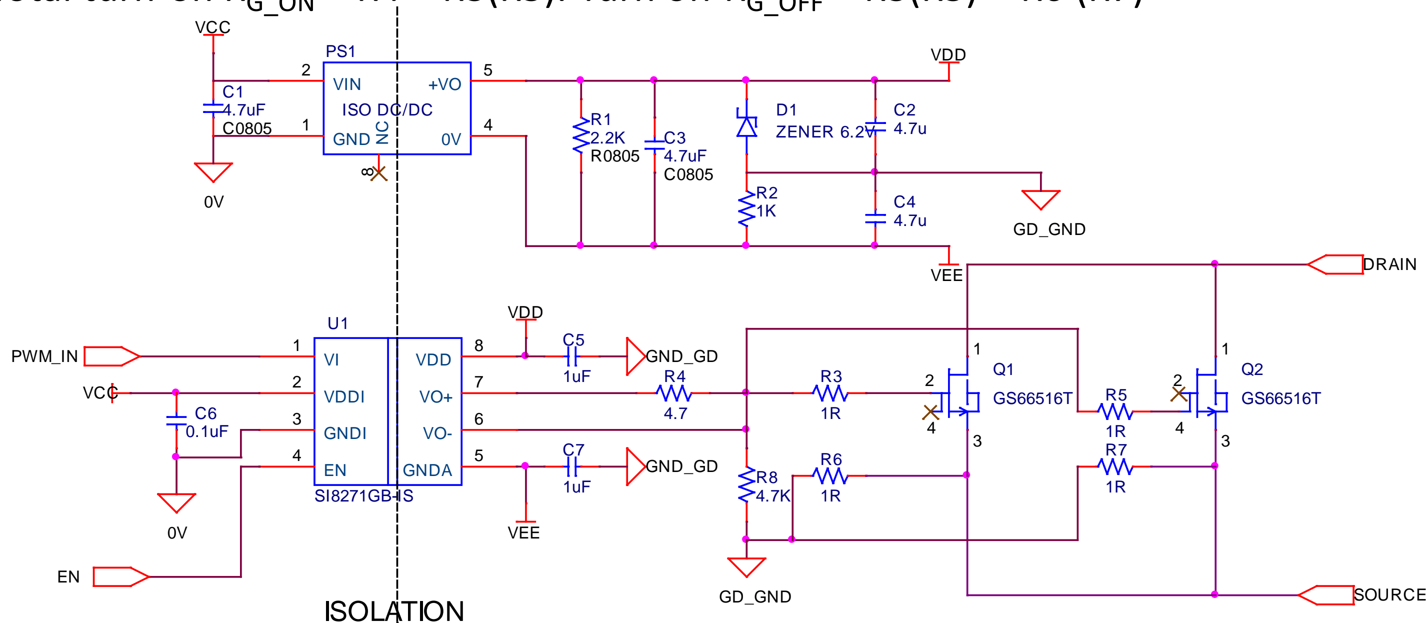
$L_{CS1\text{-}4}$: Common source inductance

- Defined as any inductance that couples power loop switching noise (L*di/dt) into the gate drive circuit
- Including the shared/common source inductance and mutual inductance between power and drive loops
- **Feedback switching di/dt to V_{GS}, impact gate drive stability and performance**
- **Minimize as much as possible.**

Gate drive design for paralleled GaN

GaN Systems

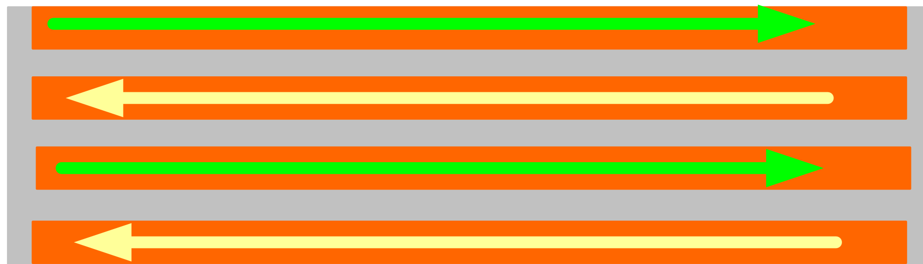
- For high current paralleling design, a small negative gate drive turn-off bias is recommended for lower turn-off loss and more robust gate drive. Recommend to use -3V to -5V with synchronous driving for optimum efficiency.
- Create bipolar gate drive from single power supply using a 6.2V Zener. Negative gate drive bias (VEE) is defined by PS1 output – Vzener(6V)
- Use small values (1-2Ω) for distributed gate and source resistance: R3/R5 and R6/R7
- Total turn-on R_{G_ON} = R4 + R3(R5). Turn off R_{G_OFF} = R3(R5) + R6 (R7)

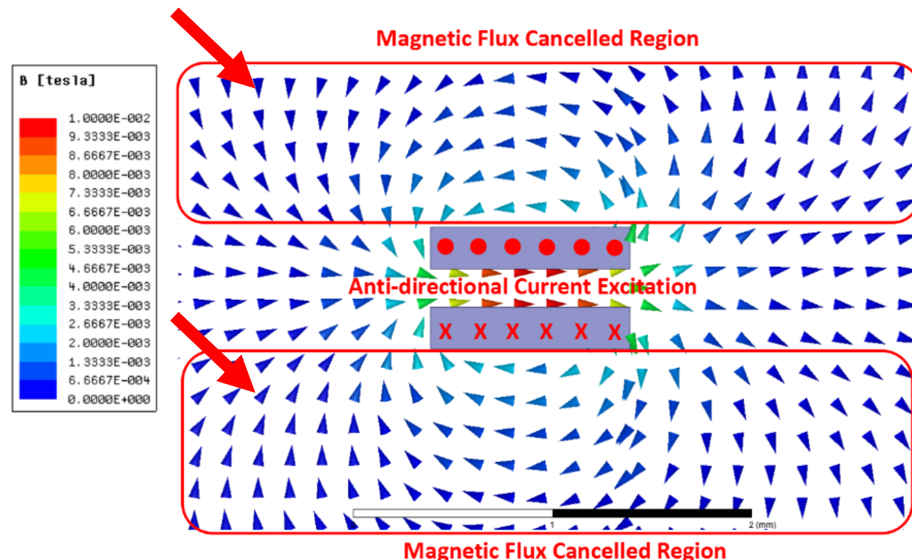


Flux cancelling for lower inductance

GaN Systems

- When two adjacent conductors are located close with opposite current direction, magnetic flux generated by two current flows will cancel each other in the region highlighted.
- This magnetic flux canceling effect can lower the parasitic inductance.
  - Arrange the layout so that high-frequency current flows in opposite direction on two adjacent PCB layers

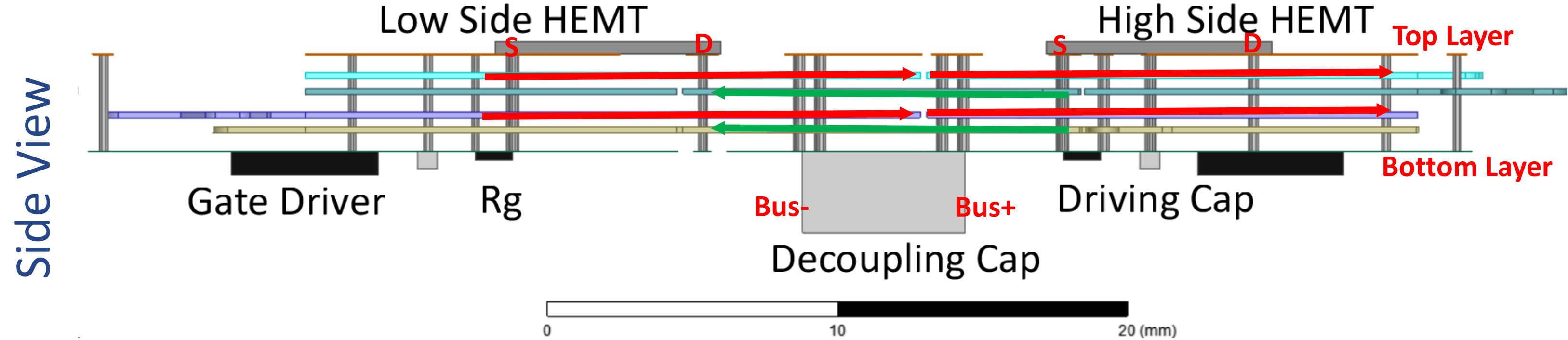


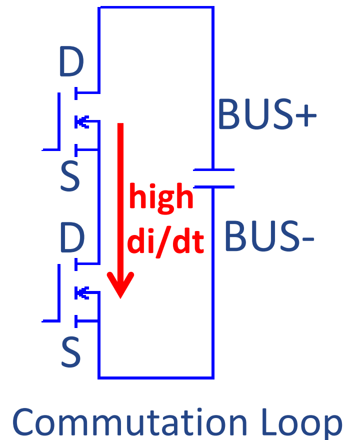


Flux Cancelling Design for half bridge layout

GaN Systems

Side View





Commutation Loop

High Frequency Current alternates direction on Each Layer to provide flux canceling effect

Top Layer: place GaN HEMTs

Mid_L1: BUS+ -> Drain_High ; Source_Low -> BUS-

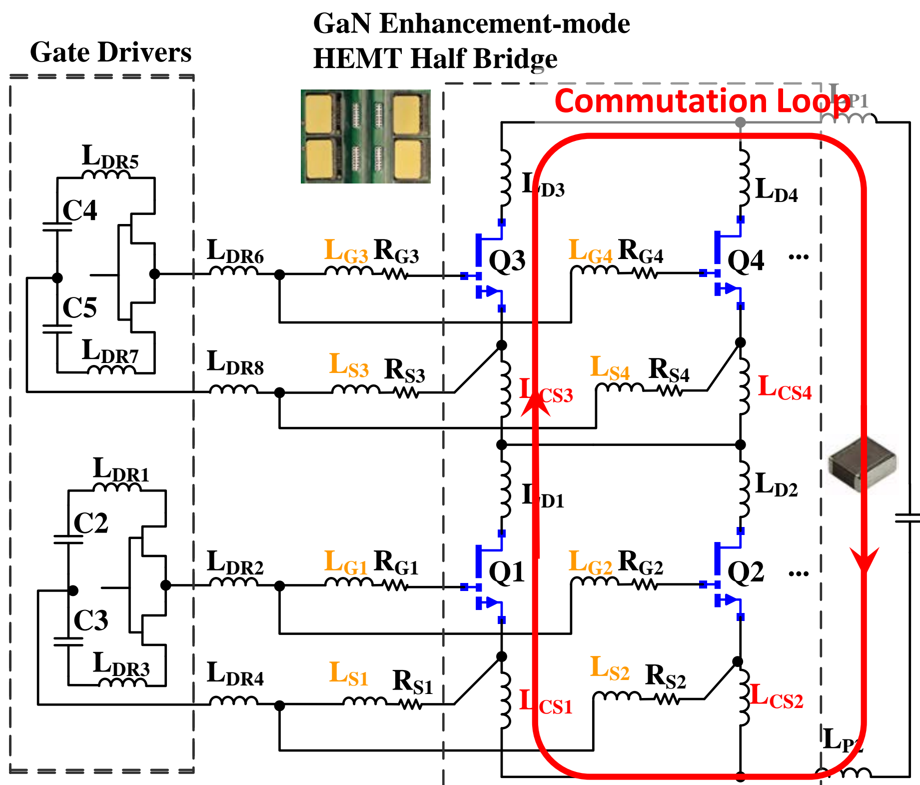
Mid_L2: Source_High -> Drain_Low

Mid_L3: BUS+ -> Drain_High ; Source_Low -> BUS-

Mid_L4: Source_High -> Drain_Low

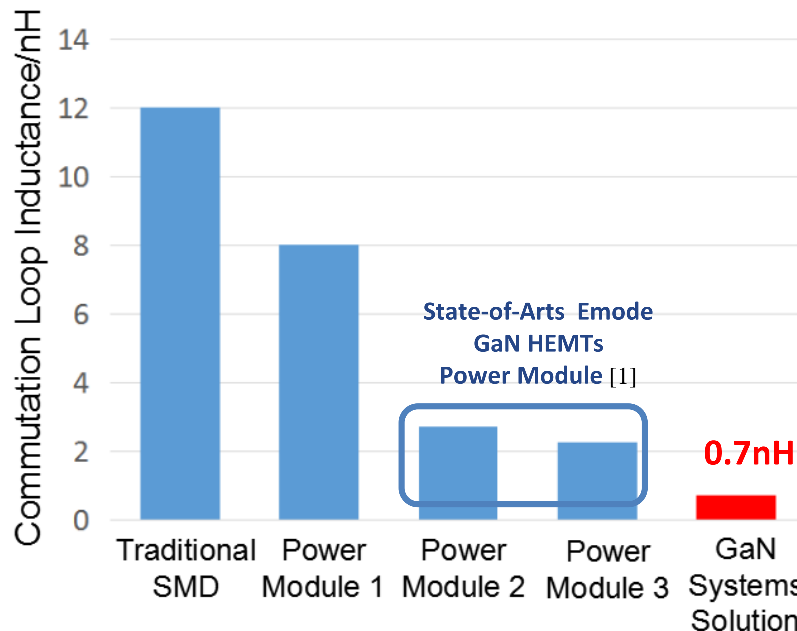
Bottom Layer: place Gate Driver Circuit and Decoupling Caps

Comparison with Benchmark



GaN Systems Solution: only 25% L_{Loop} of the Best Counterparts:

- Low inductance GaN*PX*® package
- Flux cancelling PCB design



[1] F.Luo, Z.Chen, L.Xue, P.Mattavelli, D.Boroyevich, B.Hughes, "Design Considerations for GaN HEMT Multichip Half- bridge Module for High-Frequency Power Converters"

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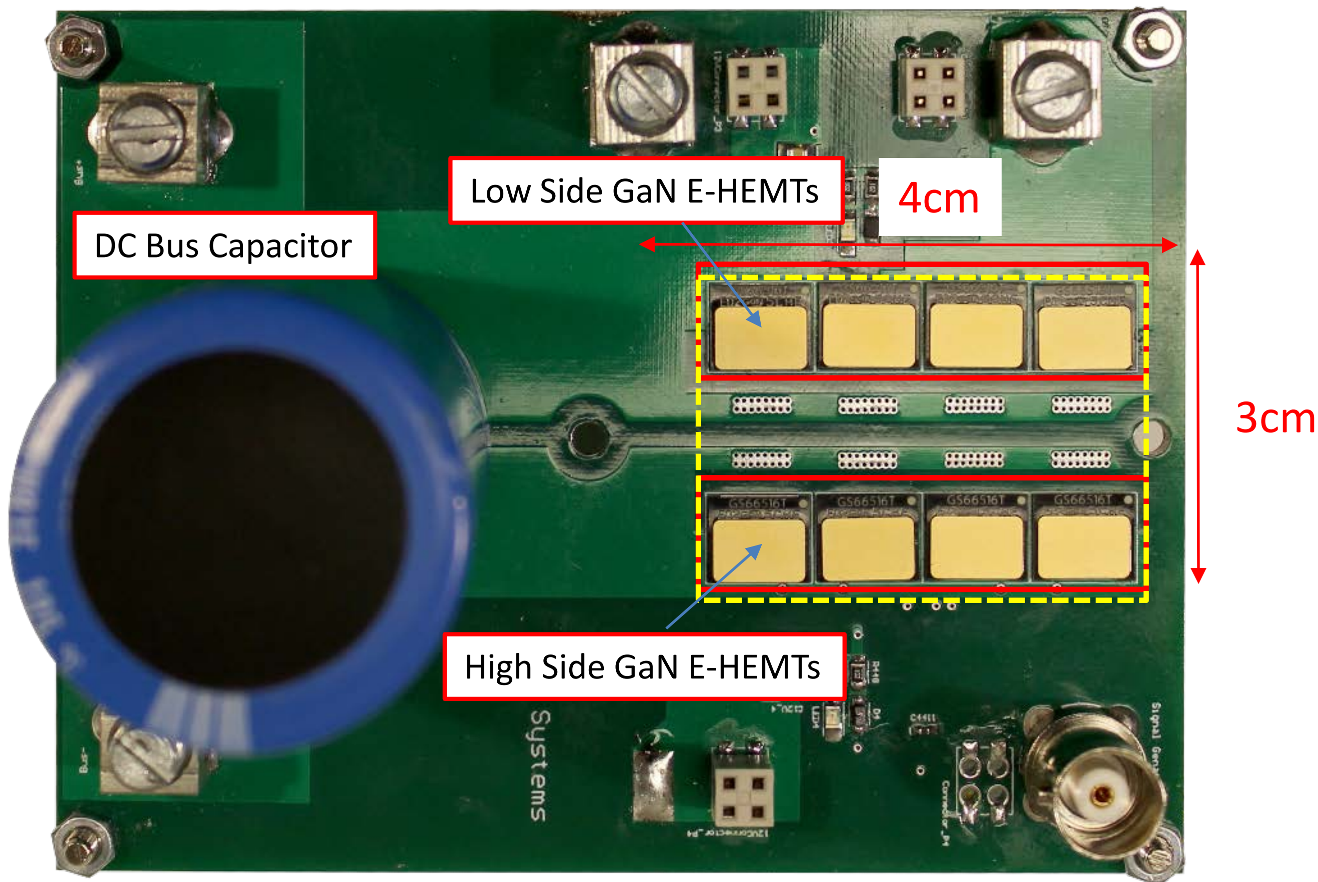
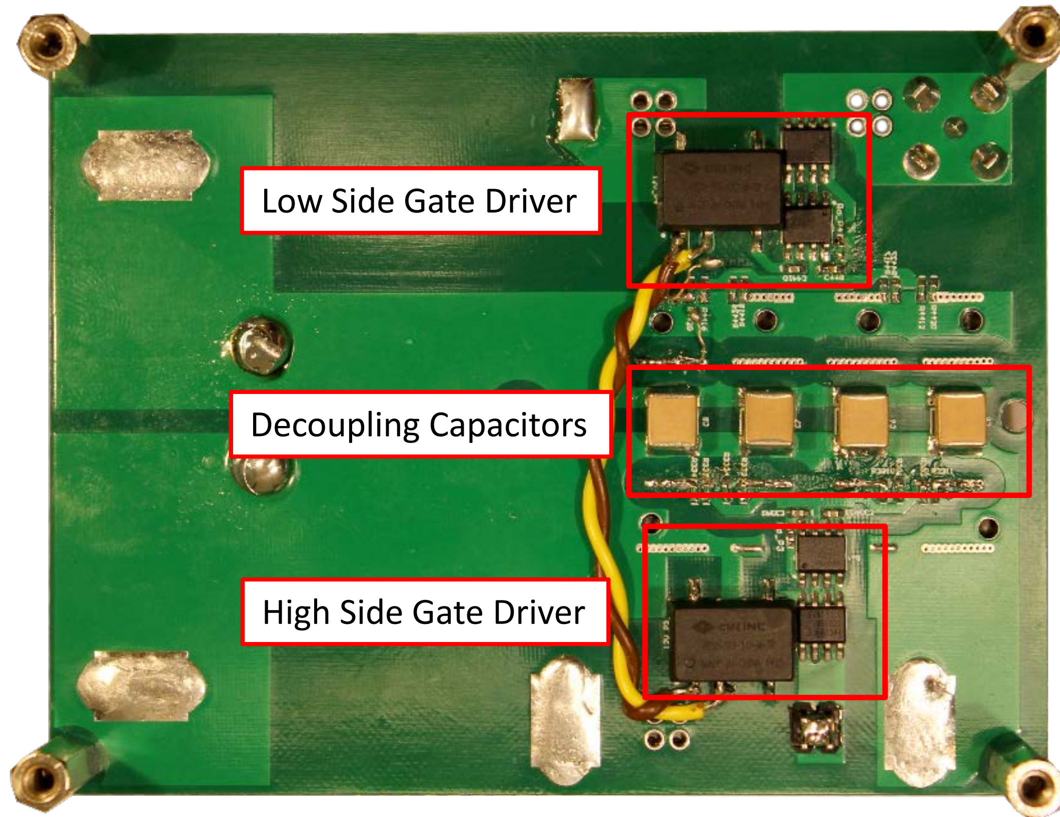
4x GS66516T Paralleling Test Board – Top View

650V/240A high Power stage design using discrete GaN EHEMTs

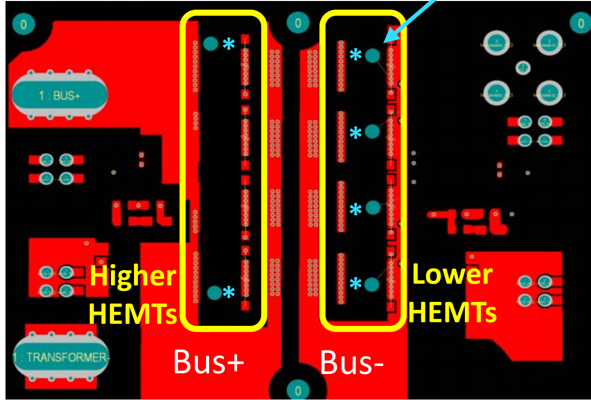


4x GS66516T Paralleling Test Board – Bottom View

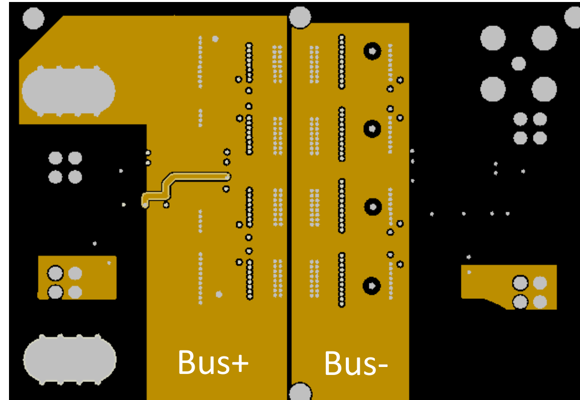


Layout of 4x paralleled GaN power stage

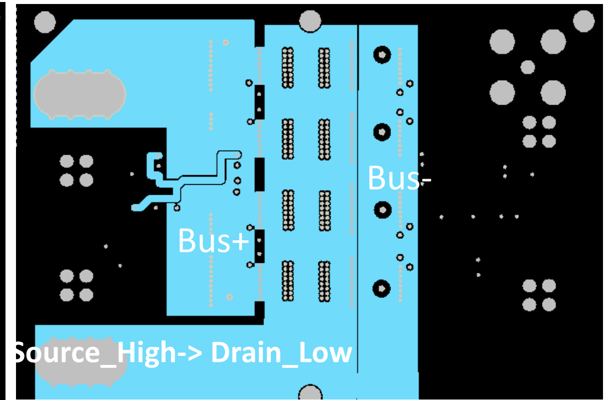
* Un-plated holes, for thermal measurement. Avoid routing electrical signals under the device.



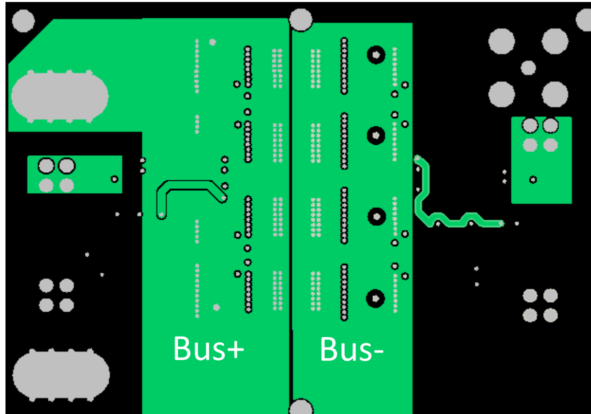
Top Layer



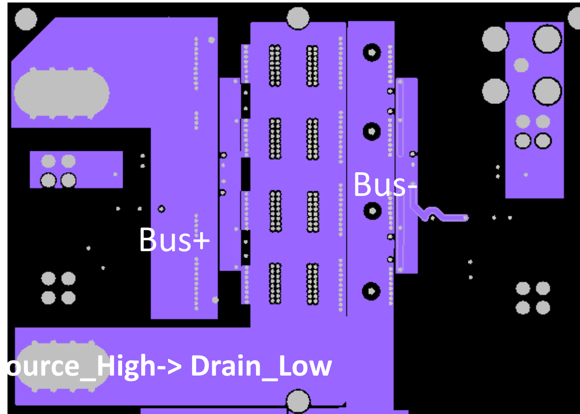
Mid_L1



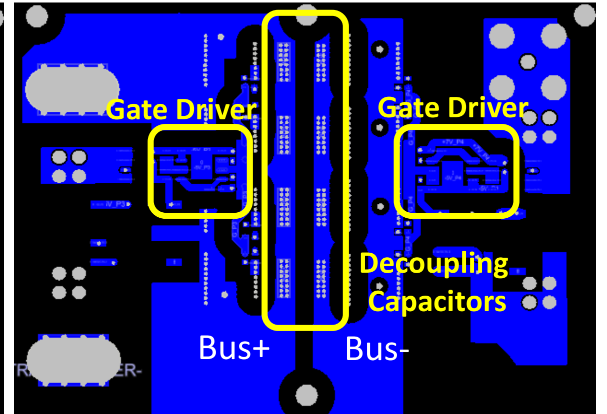
Mid_L2



Mid_L3



Mid_L4



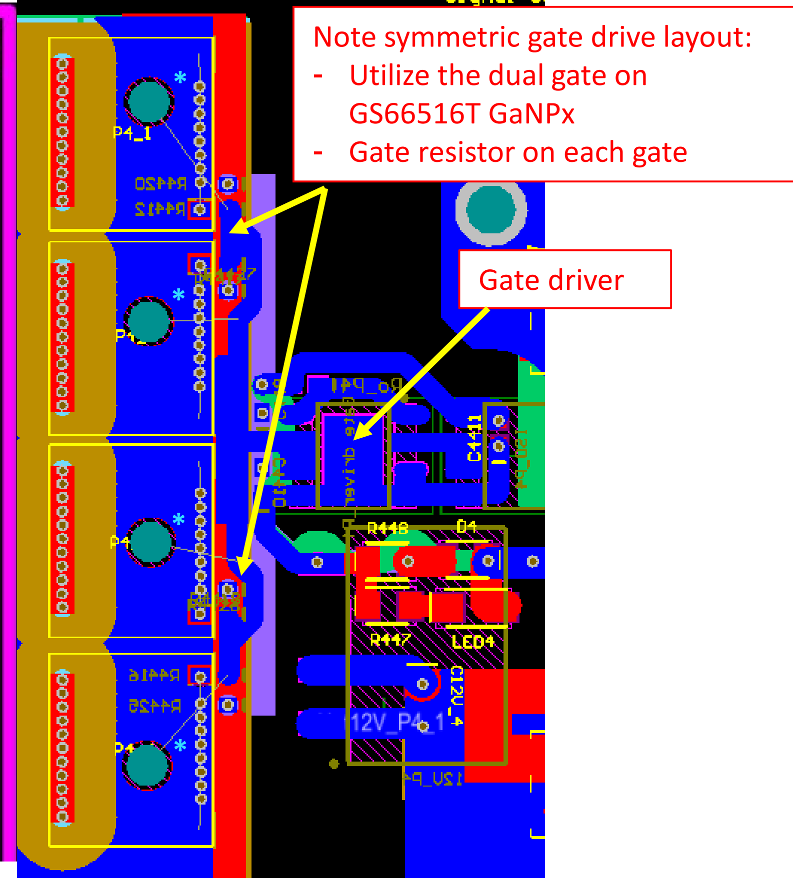
Bottom Layer

Optimum Paralleling Layout for GaN HEMT (4x GS66516T)

GaN Systems

Top side with 4x GS66516T in half bridge

Bot side with gate driver



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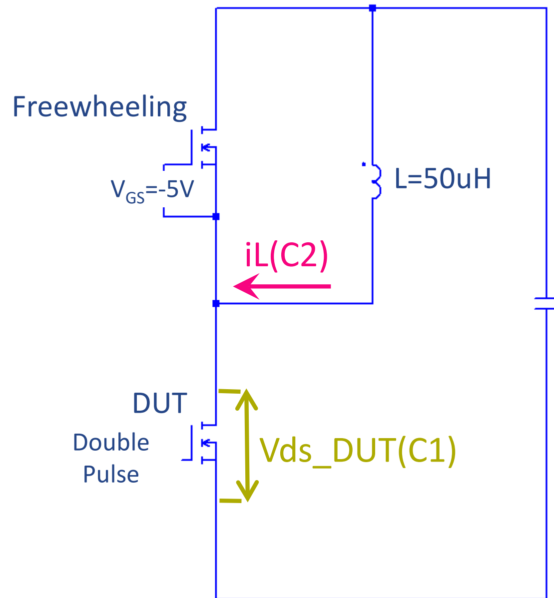
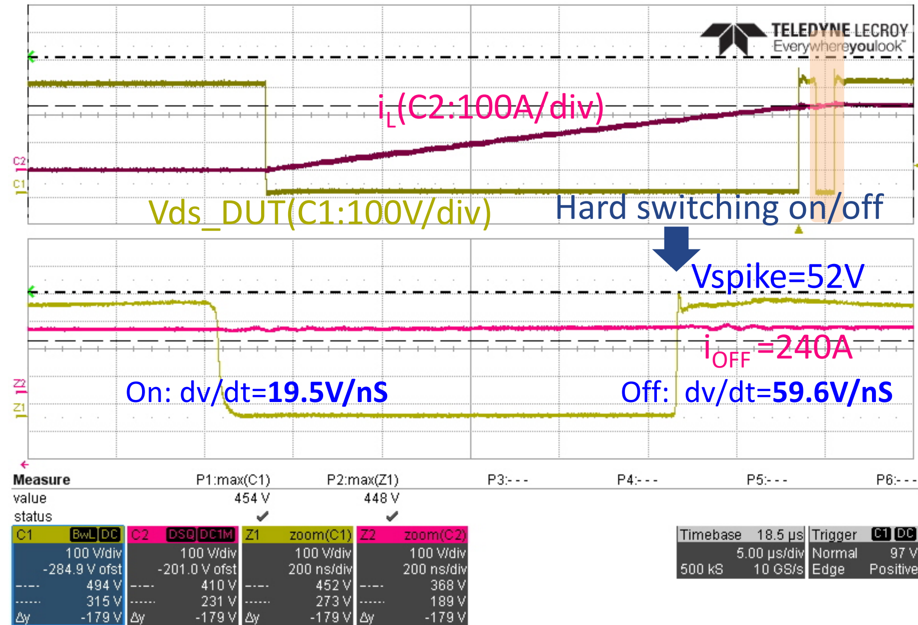
400V/240A double pulse hard Switching test waveforms

DUT: 4x GS66516T in parallel; Freewheeling: 4x GS66516T in parallel

Condition: V_{BUS}=400V, I_{DS_ON}=231A, I_{DS_OFF}=240A, V_{GS}=+6.8V/-5V, R_{G_ON}=4.55ohm, R_{G_OFF}=1.25 ohm.





Measurement Setup: Lecroy WaveSurfer 10M Oscilloscope, HVD3106 Differential Probe(C1), CWT-3LFB mini Rogowski Coil(C2)

Experimental Waveform

- ***No-Derating Paralleling of GaN HEMTs. Hard switched up to full rated current with clean waveform.***
- ***400V/240A Hard Switching Capability with ~200V V_{DS} Margin***

Summary

GaN Systems

- Paralleling discrete GaN is desired to achieve higher power output
- GaN Systems E-HEMT device characteristics are inherently fit for paralleling:
  - Positive $R_{DS(ON)}$ temperature coefficient
  - Stable gate threshold over the temperature range
  - Negative tempco of g_m
  - Low inductance GaN*PX*® package for minimum circuit mismatch

- Layout is critical for paralleling high speed GaN HEMT:
  - Low and balanced parasitic inductance on the power and gate drive loop. Equal length of gate drive layout and optimum gate driver circuit

- Summary
  - Provided practical design guide on how to parallel high speed GaN HEMT devices
  - Showed a design layout example of 4x paralleled GaN E-HEMT half bridge power stage
  - Hardware was built and GaN E-HEMT paralleled operation has been validated up to the rated current under hard switching test (400V/240A)