An Experimental Comparison of GaN E-HEMTs versus SiC MOSFETs over Different Operating Temperatures

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***Abstract*— Research on wide bandgap (WBG) devices has been conducted for many years. The reason that the properties of Gallium Nitride (GaN) and Silicon Carbide (SiC) excite power engineers is because they show substantial performance improvements over their silicon-based counterparts. In this paper, a fair comparison test platform with closed-loop junction temperature control function is introduced to compare switching performance and temperature-dependent switching energy between a 650 V/30 A GaN E-HEMT and a 900 V/35 A SiC MOSFET. Meanwhile, a synchronous buck converter is configured to compare system efficiency and junction temperature in real switching application. The experimental results are consistent with theoretical analysis.**

***Keywords— wide band gap,* GaN E-HEMTs, SiC MOSFETs, double pulse test, temperature dependent, switching energy loss Eon/Eoff**

I. INTRODUCTION

Both GaN and SiC have material properties superior to Si for switching power devices. WBG devices offer five key characteristics, including high dielectric strength, high-speed switching, tolerance of high operating temperature environments, high current density, and low on-resistance. WBG devices have been emerging quickly and applied in various power electronics applications, e.g., onboard electric vehicle battery chargers, motor control, energy storage systems, travel adapters, wireless chargers, smart home appliances and high efficiency AC-DC data center power supplies.

Many manufacturers offer WBG components in a vast variety which are difficult to keep track of. Researchers and engineers need to navigate the available options in order to choose the right devices. Before a power engineer designs a power converter, one critical step is to conduct a power loss analysis of the system. According to the power loss analysis, engineers can estimate system efficiency. The power switching device's loss must be factored into the total loss of the system. The losses can be broken down into switching loss, conduction loss, deadtime loss and gate drive loss. The switching loss includes turn-on loss and turn-off loss, which can be calculated using switching energy Eon and Eoff. GaN E-HEMTs and SiC MOSFETs have been shown to experience variable switching losses at elevated junction temperatures. This phenomenon can be explained based on the relationship between the device junction temperature and the transconductance. The temperature-dependent feature of switching loss should also be considered in the power converter design.

There should be one easy and accurate method to control junction temperature from low to high when measuring Eon and Eoff with a double pulse tester. However, according to previous literature [1], it is very challenging to perform DPT at elevated junction temperatures due to the small packaging commonly used for GaN and SiC that are difficult to heat. Some engineers customize a copper bar connection between the power device and a hot plate to heat up the junction. The drawback of this method is there is no closed-loop temperature control on the DUT's junction which results in an unstable junction temperature caused by air flow. Another method is placing the entire circuit board in an oven to heat up the devices. This method may affect the function of other components as well as the accuracy of test probes.

Due to the complexity of designing an appropriate and fair comparison test platform with a closed-loop junction temperature control function, very few publications present reliable experimental data comparing GaN E-HEMTs and SiC MOSFETs switching performance, thermal characterization of switching energy, thermal performance, system efficiency, as well as other parameters.

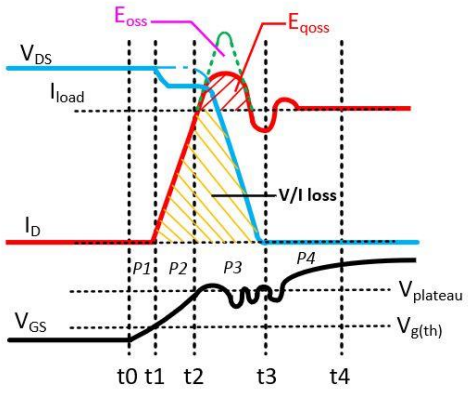
This paper first presents a theoretical analysis that details the GaN hard-switch half-bridge turn-on and turn-off

process, temperature-dependent switching loss analysis, and Q_{oss}/Q_{rr} loss differences between GaN and Si/SiC MOSFET in Section II. Then, in Section III, a novel test platform with a closed-loop junction temperature control function is introduced and configured as a double-pulse tester and DC-DC synchronous buck converter. This platform is used to empirically compare the performance of a 650 V GaN E-HEMT (650 V/30 A, 50 mΩ) versus a 900 V SiC MOSFET (900 V/35 A, 65 mΩ) with same test conditions. Finally, conclusions are given in Section IV.

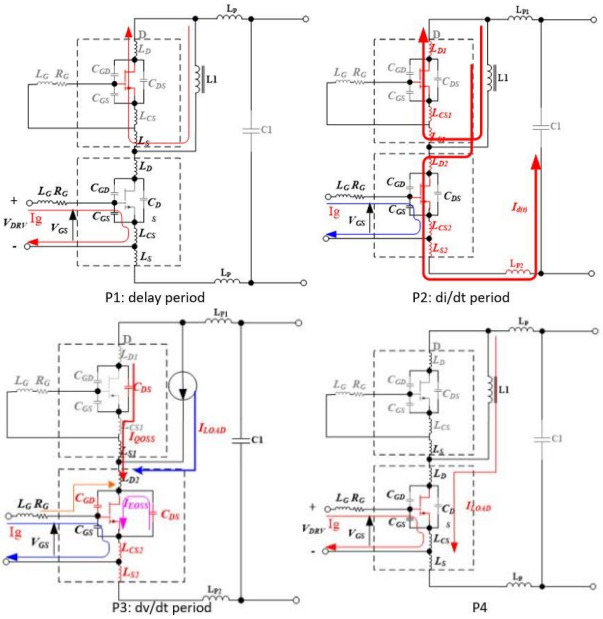
II. THEORETICAL ANALYSIS OF THE SWITCHING PROCESS

Since many papers have already introduced the SiC MOSFETs hard-switched half-bridge turn on/off analysis, this part only focuses on GaN E-HEMTs switching performance and the impact of circuit parasitics. Circuit parasitics and gate driver circuits play an important role in the switching process. The turn-on gate voltage threshold of GaN E-HEMTs is relatively low, e.g. 1.3~1.7 V, making it very sensitive to the high di/dt and dv/dt during the switching process. If V_{GS} exceeds 10V, such a device will be destroyed. As a result, considering the electrical stress caused by parasitics, more circuit layout attention is needed.

A half-bridge configuration consisting of two GaN HEMTs is shown in *Fig. 1*, in which a detailed hard-switching turn-on process is analyzed. The turn-on switching period is divided into four intervals, P1-delay period, P2-di/dt period, P3-dv/dt period and P4-remaining switching period [2] [3].



(a)



(b)

Fig. 1. Hard-switching turn-on of GaN HEMTs (a) transition waveform, (b) detailed turn-on process

P1-Delay period (t0-t1):

At t0, gate current I_G starts to charge C_{iss} exponentially. V_{GS} reaches threshold $V_{g(th)}$ at t1. When $V_{GS} < V_{g(th)}$, two-dimensional electron gas (2DEG) of GaN E-HEMTs is off, there is no drain-to-source current. GaN has very low C_{iss}, which results in a low gate driver loss and short delay time. It is important to keep gate inductance L_G low to reduce ringing and overshoot.

P2-di/dt period (t1-t2):

As $V_{GS} > V_{g(th)}$, the impedance of 2DEG begins to decrease, and drain current I_D starts to rise. I_D reaches the inductor load current at t2. The GaN device is operated in the saturation region. This region generates V/I overlapping switching loss. The overlapping switching loss of this region increases with higher junction temperature. The root cause is that transconductance of GaN E-HEMTs decreases with increased junction temperature, as shown in *Fig. 2*. This can be explained using equation (1):

$$V_{plat} = V_{g(th)} + \frac{I_d}{g_m} \quad (1)$$

Here V_{plat} is Miller plateau voltage, g_m is transconductance. With higher junction temperature Tj,

g_m decreases and thus causing higher V_{plat}, which means it takes more time for V_{GS} to reach V_{plat}, resulting in a slower slew rate di/dt and larger switching loss in this region.

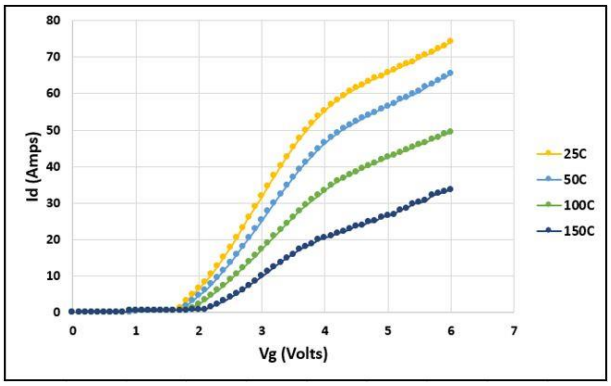


Fig. 2. Transfer characteristics at V_{ds}=9V of GS66508T.

P3-dv/dt period (t2-t3):

At t2, the drain current I_D passes I_{LOAD} and continues to rise. The output capacitance C_{oss} of the low side GaN E-HEMT begins to discharge through 2DEG internally (E_{oss} loss). Meanwhile, I_D charges the high side C_{oss} (E_{qoss} loss) and V_{DS} starts to fall. Also, this region generates V/I overlapping switching loss.

During this dv/dt period, the gate drive current I_g is shown in (2):

$$I_g = \frac{V_{drv} - V_{plat}}{Rg} \quad (2)$$

Here V_{drv} is gate drive voltage, and R_g is gate resistor. With higher junction temperature I_g decreases, since V_{plat} increases with higher Tj as mentioned above. The period of Miller plateau voltage is shown as (3):

$$t_{plat} = \frac{Q_{gd}}{I_g} \quad (3)$$

Here Q_{gd} is gate-to-drain charge. The period of Miller plateau voltage is longer with higher Tj since gate drive current I_g decreases. With a longer Miller plateau period, the slew rate of dv/dt decreases, resulting in larger overlapping switching loss in this region under higher junction temperature.

Based on the above analysis of turn-on process, the real total turn-on switching loss includes three parts as shown in (4):

$$E_{on\_real} = E_{VIon} + E_{qoss} + E_{oss} \quad (4)$$

However, the measured total turn-on loss includes only two parts as shown in (5). This is because the output capacitance C_{oss} discharges through internal 2DEG and the discharging current can't be measured directly in the test.

$$E_{on\_measured} = E_{VIon} + E_{qoss} \quad (5)$$

- Turn-off Process

The turn-off process is shown in *Fig. 3*. It includes three intervals: P1-delay period, P2-2DEG loss period, and P3-C_{oss} charging period.

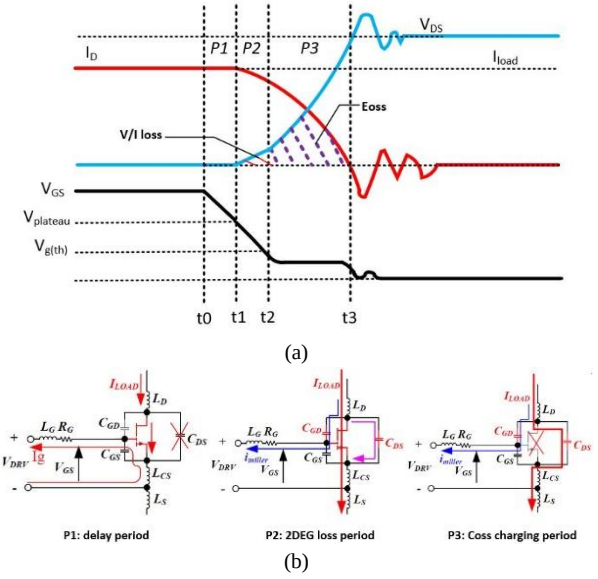


Fig. 3. Hard-switching turn-off of GaN HEMTs (a) transition waveform, (b) detailed turn-off process

P1-Delay period (t0-t1):

At t0, the gate current I_G starts to discharge input capacitance C_{iss} exponentially. There is almost no turn-off switching loss in this region. The load current I_{Load} continues to flow through 2DEG, and there is no current flowing into output capacitance C_{oss} as shown in *Fig. 3 (b)*.

P2-2DEG loss period (t1-t2):

At t2, V_{GS} drops to threshold voltage $V_{GS(th)}$, and 2DEG of GaN E-HEMT turns off. In this period, with increasing impedance of 2DEG, drain current I_D starts to redirect into C_{oss}. Most loss in this region is V/I overlapping switching loss E_{VIoff}. When the junction temperature increases, Miller plateau voltage is larger, and the 2DEG is turned off faster, therefore switching loss E_{VIoff} decreases with higher junction temperature.

However, the measurement shows the temperature-dependent feature of E_{VIoff} is not obvious. This is due to the ultra-fast transition of GaN E-HEMT, switching loss E_{VIoff} can be very small. If a larger turn-off gate resistor R_{goff} is used, the temperature-dependent phenomenon of E_{VIoff} will be observed.

P3-C_{oss} charging period (t2-t3):

From t2 gate-to-source voltage V_{GS} drops below threshold voltage $V_{GS(th)}$, the 2DEG is turned off completely, and all the load current is charging C_{oss} as shown in *Fig. 3 (b)*. Turn-off slew rate dv/dt is not controlled by the gate most of the time, only load current defines the dv/dt and rise time.

The real total turn-off loss is only E_{VIoff} as shown in (6). E_{oss} of P3 region is not part of the turn-off loss since V_{GS} is already below threshold voltage and 2DEG of GaN E-HEMT is completely shut off. Instead, E_{oss} will be dissipated at the next turn-on process. However, the measured total turn-off loss E_{off} includes the E_{oss} energy as shown in (7). This is because the C_{oss} charging current flows toward the outside of the device's package which will be measured in the test.

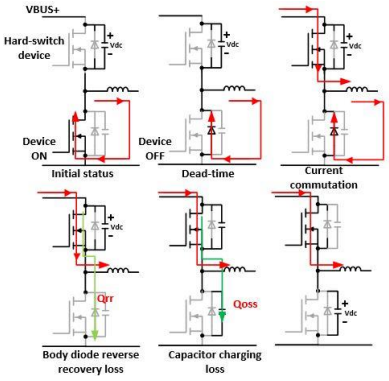
$$E_{off\_real} = E_{VIoff} \quad (6)$$

$$E_{off\_measured} = E_{VIoff} + E_{oss} \quad (7)$$

- Q_{rr} and Q_{oss} Loss at Hard-switching Turn-on

One significant difference between Si/SiC MOSFETs and GaN E-HEMTs is reverse recovery loss Q_{rr} and output capacitor charging loss Q_{oss} at hard switching turn-on process in half-bridge topology. GaN E-HEMTs doesn't have Q_{rr} since there is no body diode. However, Si/SiC MOSFETs have both Q_{rr} and Q_{oss} due to the existence of body diode. This phenomenon has been elaborated in *Fig. 4 (a) (b)* and *(c)*, synchronous buck converter. The top side device is hard switching, the bottom side device is free-wheeling. Compared with *Fig. 4 (a), Fig. 4 (b) (c)* clearly shows that in the hard switching turn on process, GaN doesn't have a reverse recovery period due to Q_{rr}.

The problem of Q_{rr} is the very high loss limits of MOSFETs in half-bridge hard switching applications. A snappy recovery body diode creates very high di/dt and thus parasitic ringing.



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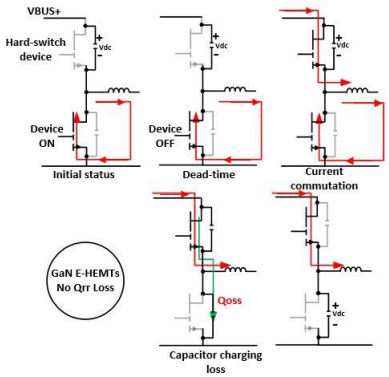

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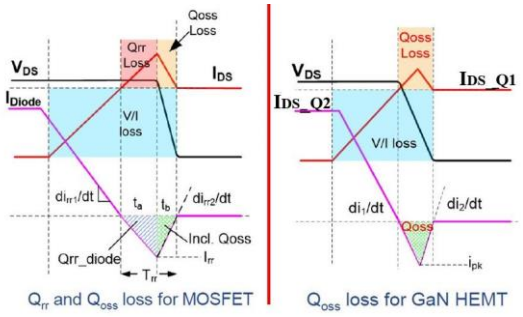


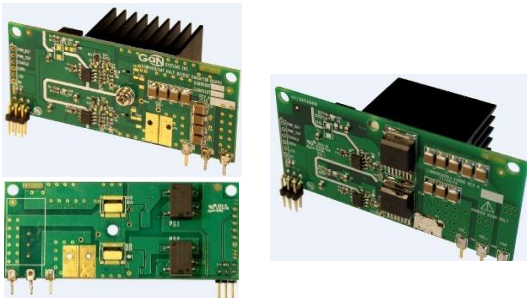
(c)

Fig. 4. Synchronous Buck Converter Hard-switch Turn-on Analysis (a) Si/SiC MOSFETs Based Analysis, (b) GaN E-HEMTs Based Analysis, (c) Q_{rr} and Q_{oss} Breakdown for Si/SiC MOSFETs and GaN E-HEMTs

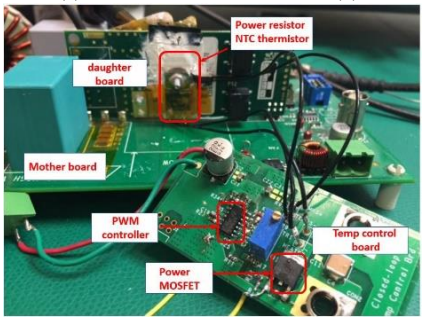
By using GaN transistors, reverse recovery effects in the converter can be eliminated and efficiency can be dramatically improved.

III. EXPERIMENTAL VALIDATIONS

For this study, the performance of a GaN transistor (650 V/30 A, 50 mΩ) was compared with a SiC MOSFET (900 V/35 A, 65 mΩ). To simplify comparing the GaN E-HEMT and SiC MOSFET, the test used a common evaluation motherboard (*Fig. 5 (c)*), paired with an interchangeable daughterboard as shown in *Fig. 5 (a) (b)*. These boards are configurable either as a buck, boost or double-pulse tester. The two daughterboards also have a very similar design. They both contain the same PCB layout, 2 oz. copper, 4 PCB layers, homogeneous thermal via and layout parasitics. The very fast switching speeds exhibited by GaN and SiC transistors require gate drivers that combine very high timing accuracy with excellent common-mode transient immunity (CMTI). To accommodate these criteria, Silicon Lab's Si8271 isolated gate driver with high CMTI was used on both daughterboards [4].



(a) (b)



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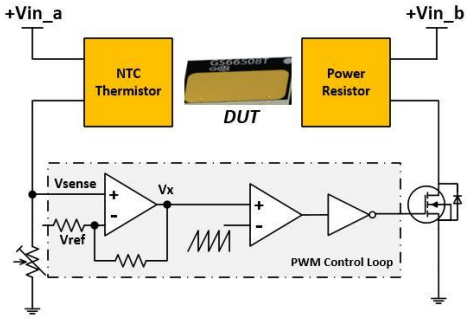

(d)

Fig. 5. Test Platform (a) GaN E-HEMT Daughter Board, (b) SiC MOSFET Daughter Board, (c) Universal Mother Board & Closed-loop Temperature Control Board, (d) Temperature Control Board Block Diagram

In order to compare the switching loss at different junction temperatures, a closed-loop junction temperature control board was designed to heat up the GaN or SiC device as shown in *Fig. 5 (c)*. The block diagram is shown in *Fig. 5 (d)*. The negative temperature coefficient (NTC) thermistor served as temperature sensor. Its resistance, 10 kΩ @ 25°C, decreased with higher temperature. The relationship between the thermistor's resistance and sensed temperature can be found from the manufacturer's datasheet. Once the targeted junction temperature is selected, a trimpot can be adjusted to reach the desired V_{sense}. When the junction temperature of DUT is lower than the setting point, the PWM controller outputs a high signal to turn on the power MOSFET to heat up DUT through the power resistor, and vice versa.

Table 1 shows the electrical characteristics of the GaN E-HEMT and SiC MOSFET. These characteristics have a major influence on the fundamental performance of the devices.

Table I: Electrical Characteristics

	GaN E-HEMT	SiC MOSFET
Package	Low inductance GaN*PX*™	D2PAK
V_{DSmax}	650 V	900 V
I_D@25°C	30 A	35 A
$R_{ds(on)}$@25°C	50 mΩ	65 mΩ
V_{GS}	-10/+7 V	-4/+15 V
C_{iss}	260 pF	660 pF
C_{oss}	65 pF	60 pF
C_{rss}	2 pF	4 pF
Q_g	5.8 nC	30.4 nC
Q_{gs}	2.2 nC	7.5 nC
Q_{gd}	1.8 nC	12 nC
Q_{rr}	0 nC	245 nC

A half-bridge, hard switching, double pulse test was conducted under 400 V/ 15 A on both GaN and SiC daughterboards. The turn-on resistor $R_{g(on)}$ was 10 Ω, while the turn-off resistor $R_{g(off)}$ was 1 Ω. The results of two double pulse switching tests follow. *Figs. 6 (a)* and *(b)* show a close-up view of the turn-on and turn-off periods, and demonstrate the switching performance of the GaN E-HEMT versus the SiC MOSFET. In the turn-on period, dv/dt for GaN reached 90 V/ns, 4X faster than the SiC 18 V/ns. In the turn-off period, dv/dt for the GaN E-HEMT performed 2X faster than the SiC MOSFET.

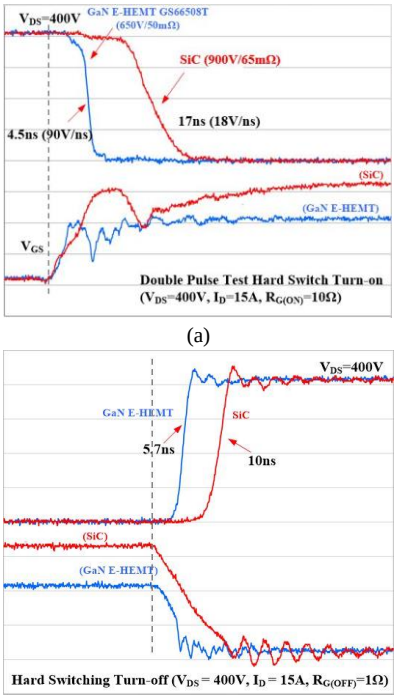

Fig. 6. Double Pulse Test Waveform (a) Hard Switch Turn-on, (b) Hard Switch Turn-off

Fig. 7 shows the switching loss measurements with a drain-to-source voltage of 400 V, drain current from 0 to 30 A for GaN and SiC. The turn-on loss dominated the overall hard switching loss. For GaN E-HEMT, Eon at 0 A is the Q_{oss} loss, caused by the C_{oss} at the high side switch. For the SiC MOSFET, Eon at 0 A is the sum of Q_{oss} loss and the reverse recovery charge Q_{rr} loss at the high side switch. Using the same test conditions, the GaN E-HEMT shows a much improved Eon/Eoff. The Eon/Eoff difference between GaN and SiC can be quantified by calculating the switching loss: $(E_{on} + E_{off}) \times f_{sw}$. For example, at 400 V/15 A, and 100 kHz, the switching loss P_{sw} of GaN is 5.217 W, while the P_{sw} of SiC is 15.211 W, ΔP_{sw}= 9.994 W. However, at 200 kHz, the P_{sw} of GaN is 10.434 W, versus a SiC P_{sw} of 30.422 W, ΔP_{sw}=19.988 W. The result, shown in *Fig. 8*, clearly shows that at higher switching frequencies, GaN provides a significant performance improvement over SiC. For instance, at 100 kHz, GaN provides a 10 W savings, but in the same system at 200 kHz, 20 W are saved.

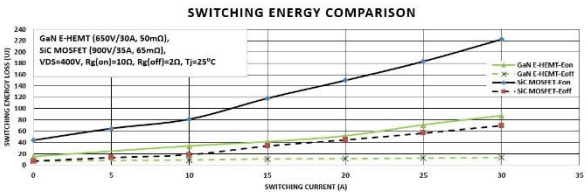

Fig. 7. Switching Energy of the GaN versus the SiC

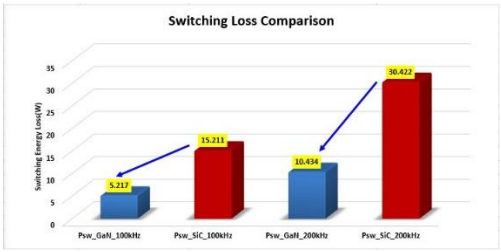

Fig. 8. 400 V/15 A GaN and SiC Switching Loss Comparison

The switching energy loss Eon/Eoff versus junction temperature between GaN and SiC was measured. The results of using a switching voltage of 400 V, a switching current ranging from 5 A to 20 A, and junction temperature ranging from 25 °C to 125 °C are shown in *Fig. 9*. From experimental results, turn-on switching loss Eon of GaN increases with higher junction temperature, and turn-off switching loss Eoff changes slightly with variable junction temperature. This result is consistent with the theoretical analysis. The Eoff temperature-dependent feature of the SiC MOSFET is not obvious according to test results. The Eon of SiC MOSFET decreases with higher junction temperature, the root cause being the transconductance g_m of the SiC MOSFET increases with higher junction temperature, which is opposite that of GaN E-HEMTs. Although the total switching loss of SiC decreases with higher Tj and the total switching loss of GaN increases with higher Tj, GaN still shows smaller switching losses compared with SiC from 25 °C to 125 °C.

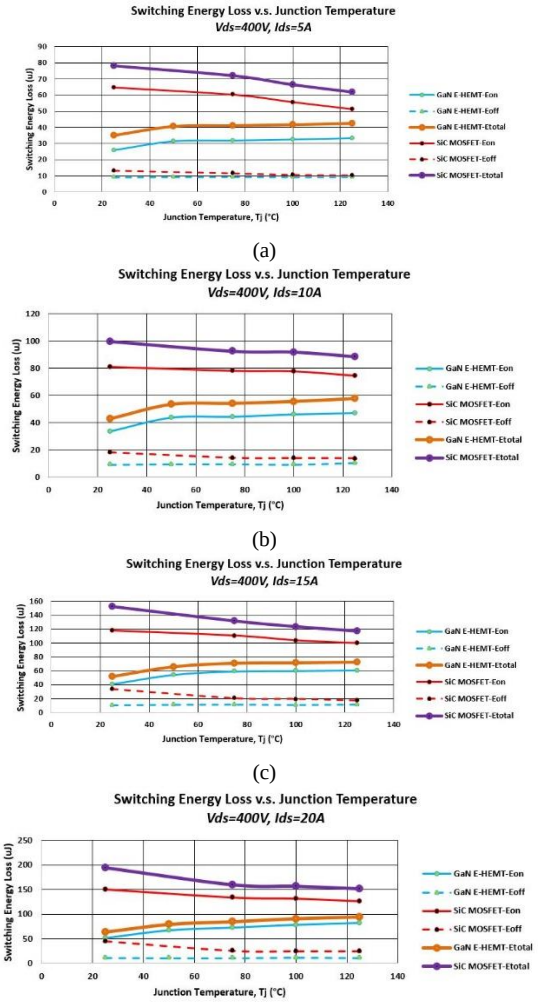

Fig. 9. Switching Energy Loss E_{on}/E_{off} versus Junction Temperature (a) V_{ds}=400 V, I_{ds}=5 A (b) V_{ds}=400 V, I_{ds}=10 A (c) V_{ds}=400 V, I_{ds}=15 A (d) V_{ds}=400 V, I_{ds}=20 A

To measure the thermal resistance of both devices, a 35×35 mm heatsink was mounted on the bottom of both daughterboards. In addition, an electrical fan with an air flow of 12.0 CFM (0.340 m3/min) was attached to the heatsink. Using the same test conditions, the SiC measured 7.724°C / W, versus GaN of 5°C / W. The thermal resistance from junction to ambient of GaN measured 1.5X better than SiC, as shown in *Fig. 10*.

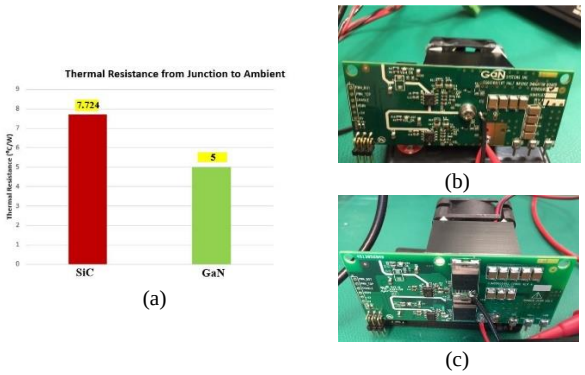

Fig. 10. Thermal Resistance Measurement from Junction to Ambient (a) *GaN vs. SiC* Measurement Result (b) GaN Thermal Resistance Setup (c) SiC Thermal Resistance Setup

A synchronous buck converter with an input voltage of 400 V and an output voltage of 200 V was tested. At a 200 kHz switching frequency, the output power varied from 100 W to 1 kW. *Fig. 11* compares the sync buck converter system efficiencies and the device's hard-switching junction temperature using GaN E-HEMTs versus SiC MOSFETs. The graph shows that the efficiency and junction temperature using GaN E-HEMTs performed better than SiC MOSFETs under the same test conditions. Power loss of the devices was equal to $\frac{Tj-T_{amb}}{Rth(JA)}$. From 0 to 1 kW, at 200 kHz GaN P_{Loss} is 45%-59% that of SiC. *Table 2* shows the performance improvement of GaN E-HEMTs over SiC MOSFETs at an output power of 900 W. At P_{out}=900 W, the Tj of the GaN E-HEMT was 59°C lower than the SiC MOSFET, and the power loss of GaN was 5.38 W lower than that of SiC. The superior performance of GaN versus SiC can be attributed to GaN's lower switching energy loss E_{on}/E_{off}. Because the conduction loss was small, the switching loss $(E_{on}+E_{off})\times f_{sw}$ accounted for over 85% of device's total power loss. Hence, as the switching frequency increases, GaN E-HEMTs will perform better than SiC MOSFETs.

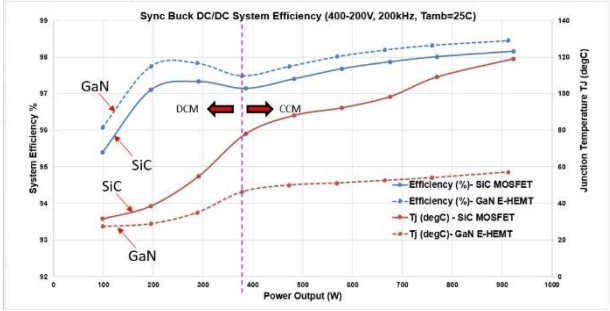

Fig. 11. Synchronous Buck DC/DC System Efficiency (400 V-200 V, 200 kHz, T_{amb}=25°C)

Table II: Power Loss and Junction Temperature Comparison at Pout=900 W, Fsw= 200 kHz

GaN has lower junction temperature and lower switching loss			
	GaN E-HEMT Solution	SiC MOSFET Solution	GaN advantage
Chip-area (mm^2)	31	160	5X smaller
Conduction Loss (W)	0.27	0.36	
Switching Loss (W)	6.1	11.4	
Total Loss (W)	6.4	11.8	~50% lower
Junction Temp. (°C)	57	116	50% lower

IV. CONCLUSIONS

This article compares the fast switching device characteristics of GaN E-HEMTs versus the best competing SiC MOSFETs. When used in synchronous buck DC/DC converter applications, the converters that use GaN E-HEMTs exhibit much higher efficiencies than ones that use SiC MOSFETs. In this application, the results clearly demonstrate that the performance of GaN E-HEMTs exceeds the performance of the best SiC MOSFETs in terms of switching speed, parasitic capacitance, switching loss and thermal characteristics. Furthermore, compared with their SiC counterparts, GaN E-HEMTs facilitate the construction of significantly more compact and efficient power converter designs.

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