



GN009 Application Note

PCB Layout Considerations with GaN E-HEMTs

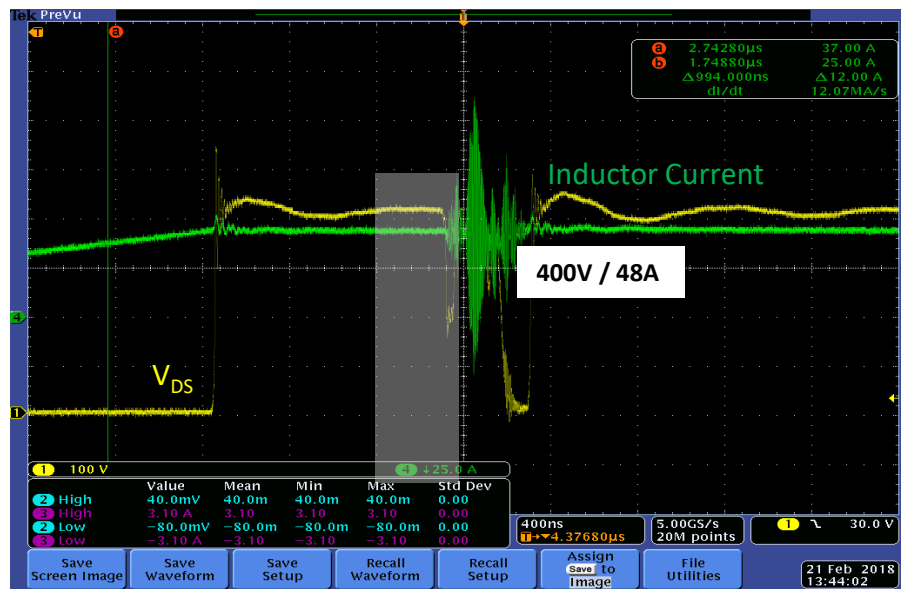
January 18, 2019

- This guide provides an overview of the good engineering practice for PCB layout of designs using GaN Systems' embedded GaNPX[®] packaged E-HEMTs.
- Layout guidelines are introduced for the following four circuit configurations
 - 1) Isolated gate driver circuit for single GaN E-HEMTs
 - 2) Isolated gate driver circuit for paralleled GaN E-HEMTs
 - 3) Half-bridge Bootstrap gate driver circuit
 - 4) EZDriveSM circuit
- With optimum board layout combined with low GaNPX[®] package inductance, GaN E-HEMTs exhibit optimum switching performance

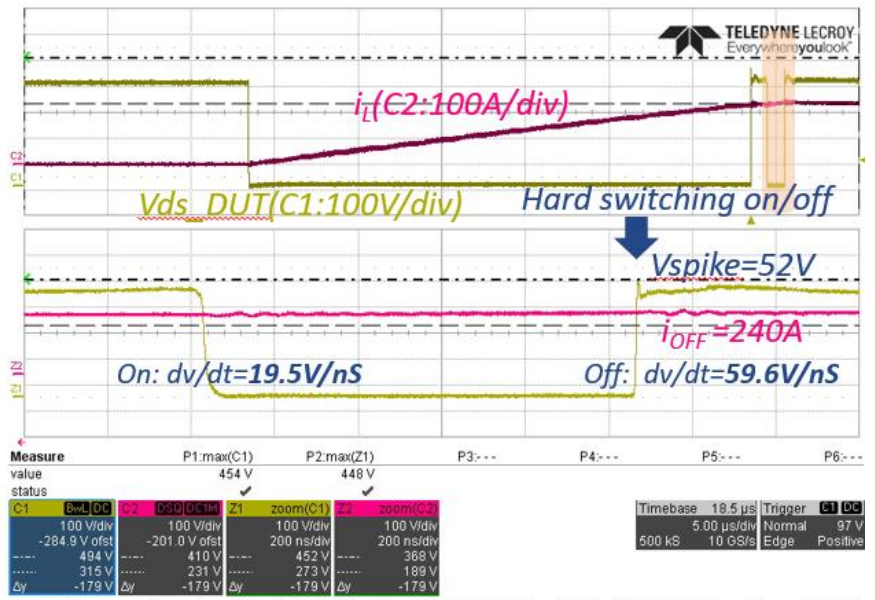
- GaN Systems' E-HEMTs have very low packaging inductance, while enabling ultra-low inductance PCB power loops.
- Good engineering practice of layout techniques are required to minimize parasitic inductance and fully utilize the benefit of GaN Systems' E-HEMTs.
- This application note shows key steps to design an optimal PCB layout with GaN to maximize converter performance.

Motivation

- GaN E-HEMTs switch much faster than Si MOSFETs, and require proper engineering consideration of PCB layout design to minimize parasitic inductances.
- Parasitic inductances can cause higher overshoot voltages, ringing/oscillation, EMC issues, which can lead to overstressing the E-HEMTs.



Example of an unsuccessful design caused by unbalanced quasi-common source inductance



Measurement Setup: Lecroy WaveSurfer 10M Oscilloscope, HVD3106 Differential Probe(C1), CWT-3LFB mini Rogowski Coil(C2)

Example of clean switching waveforms when good PCB layout practices are used (400 V/240 A DPT)

Step 1: Prepare the schematics and identify the components of each critical loop

- Isolated gate driver circuit for single GaN HEMTs
- Isolated gate driver circuit for paralleled GaN HEMTs
- Half-bridge Bootstrap gate driver circuit
- EZDriveSM circuit

Step 2: Place the components according to the design priority and current direction

- Put components as close as possible
- According to the current direction, set the component in sequence
- If there is a conflict for minimizing all the loops, refer to the priority listed on slide 7/8/9/10.

Step 3: Connect the components optimally to achieve low parasitics with flux cancellation techniques

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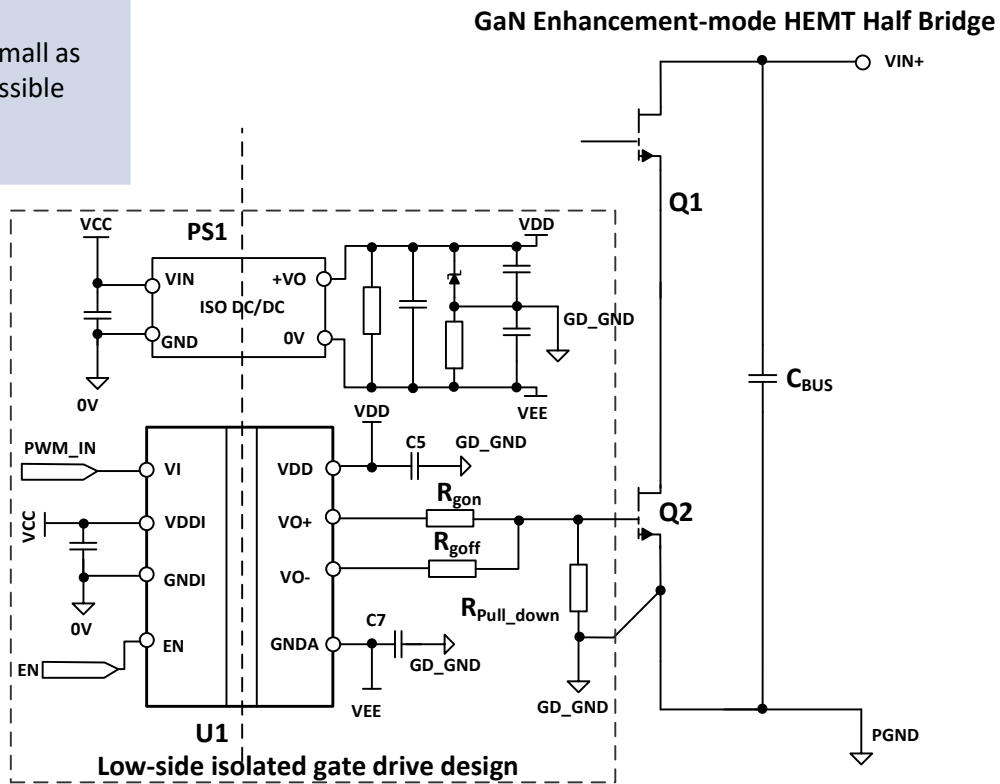
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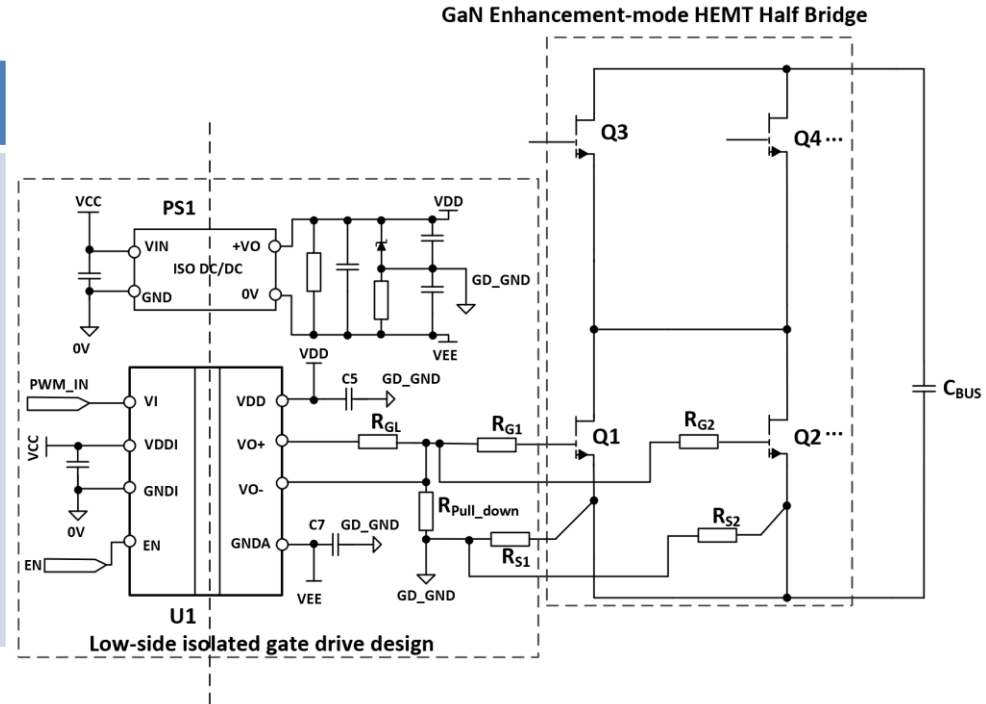
Isolated gate driver circuit for single GaN HEMT

Priority	Critical Loops	Components	Critical Loops Design Rule
1	Power Commutation loop	Q1,Q2,C _{BUS}	As small as possible
2a	LS Gate Driver loop (turn-on)	C5,U1,R _{gon} ,Q2	
2b	LS Gate Driver loop (turn-off)	C7,U1,R _{goff} ,Q2	

- High-side isolated gate drive design is symmetric as Low-side, not shown in the diagram
- Priority of HS gate driver loop is same as LS



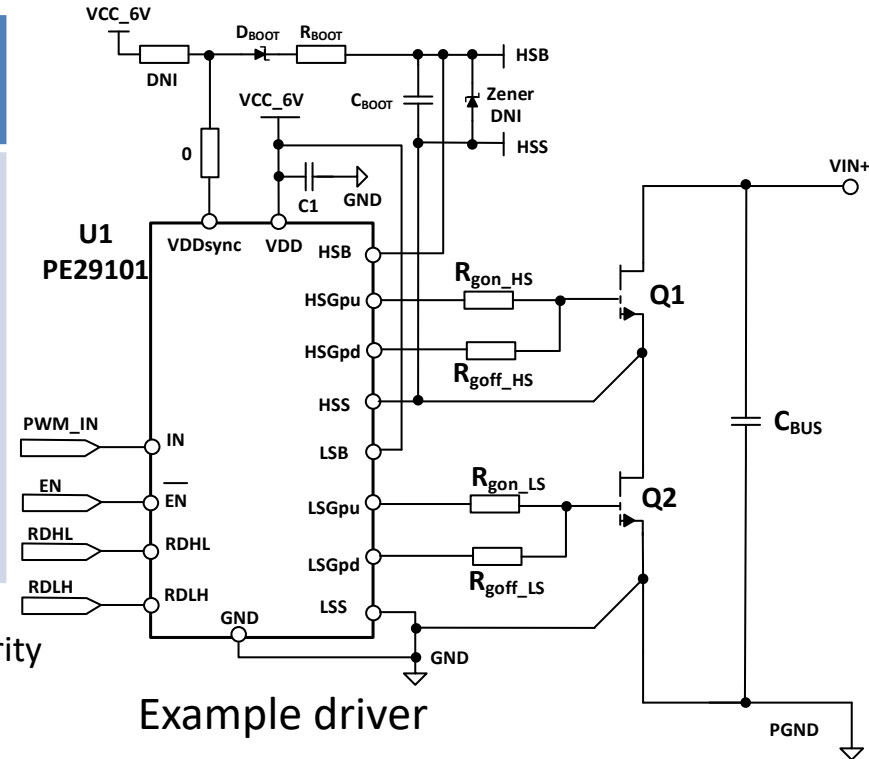
Priority	Critical Loops	Components	Critical Loops Design Rule
1a	Quasi-common source loop (high-side)	Q3, Q4	As small and symmetric for each of paralleled devices as possible
1b	Quasi-common source loop (low-side)	Q1, Q2	
2	Power Commutation loop	C _{BUS} , Q3/Q4, Q1/Q2	
3a	LS Gate Driver loop (turn-on)	C5, U1, R _{GL} , R _{G1} /Q1/R _{S1} , R _{G2} /Q2/R _{S2}	
3b	LS Gate Driver loop (turn-off)	C7, U1, R _{G1} /Q1/R _{S1} , R _{G2} /Q2/R _{S2}	



- High-side isolated gate drive design is symmetric as Low-side, not shown in the diagram
- Priority of HS gate driver loop is same as LS
- **Distributed gate and source resistance R_{G1}/R_{G2} and R_{S1}/R_{S2} needs to be separated**

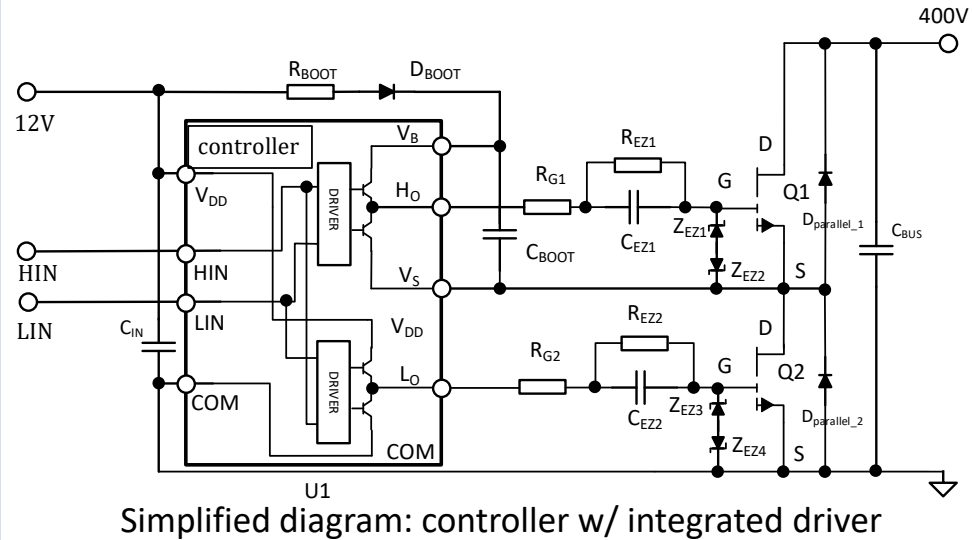
Half-bridge Bootstrap Gate Driver Circuit (Non-isolated)

Priority	Critical Loops	Components	Critical Loops Design Rule
1	Power Commutation loop	Q1, Q2, C _{BUS}	As small as possible
2a	HS Gate Driver Loop (turn-on)	D _{BOOT} , R _{BOOT} , C _{BOOT} , U1, R _{gon_HS} , Q1	
2b	HS Gate Driver Loop (turn-off)	Q1, R _{goff_HS} , U1	
2c	LS Gate Driver Loop (turn-on)	C1, U1, R _{gon_LS} , Q2	
2d	LS Gate Driver Loop (turn-off)	Q2, R _{goff_LS} , U1	



- Use above table to identify critical loop, components and priority

Priority	Critical Loops	Components	Critical Loops Design Rule
1	Power Commutation Loop	Q1, Q2, C _{BUS}	As small as possible
2a	HS Gate Driver Loop (turn-on)	R _{BOOT} , D _{BOOT} , C _{BOOT} , U1, R _{G1} , R _{EZ1} , C _{EZ1} , Z _{EZ1} , Z _{EZ2} , Q1	
2b	HS Gate Driver Loop (turn-off)	Q1, Z _{EZ1} , Z _{EZ2} , R _{EZ1} , C _{EZ1} , R _{G1} , U1	
2c	LS Gate Driver Loop (turn-on)	U1, R _{G2} , R _{EZ2} , C _{EZ2} , Z _{EZ3} , Z _{EZ4} , Q2	
2d	LS Gate Driver Loop (turn-off)	Q2, Z _{EZ3} , Z _{EZ4} , R _{EZ2} , C _{EZ2} , R _{G2} , U1	



- Use above table to identify critical loop, components and priority

Note: more details about EZDriveSM is available from the link:

https://gansystems.com/wp-content/uploads/2018/12/GN010-EZDrive-Solution-for-GaN-Systems-E-HEMTs-_20181221.pdf

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Step 2: Place the components according to the design priority and current direction

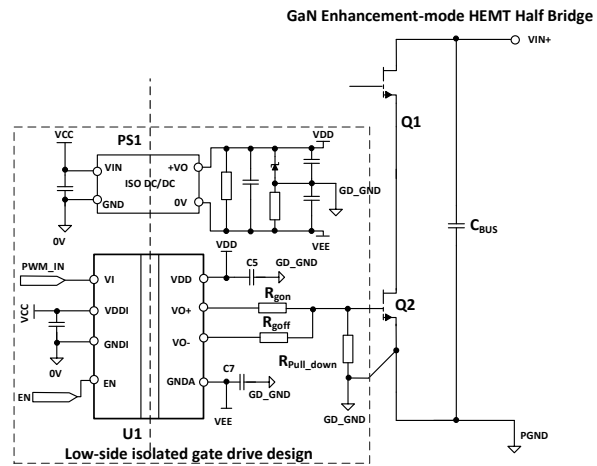
- Put components as close as possible
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- If there is a conflict for minimizing all the loops, refer to the priority listed on slide 7/8/9/10.

Step 3: Connect the components optimally to achieve low parasitics with flux cancellation techniques

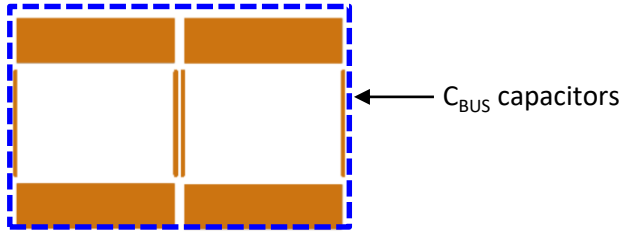
Step 2.1: Power commutation loops (Top-side cooling)

Example: Isolated gate driver circuit w/ single GaN HEMT

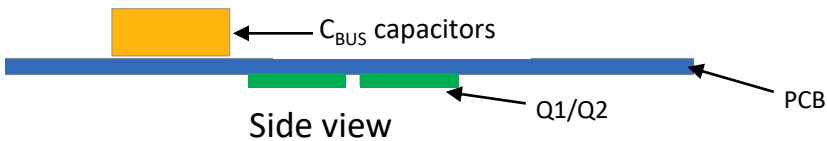
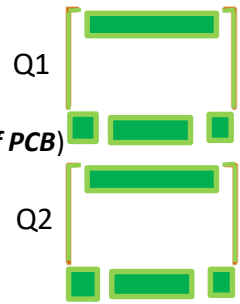
- Place components as close together as possible



Component Placement



Top-side cooled devices
(GaN HEMT Q1/Q2 are on the bottom side of PCB)

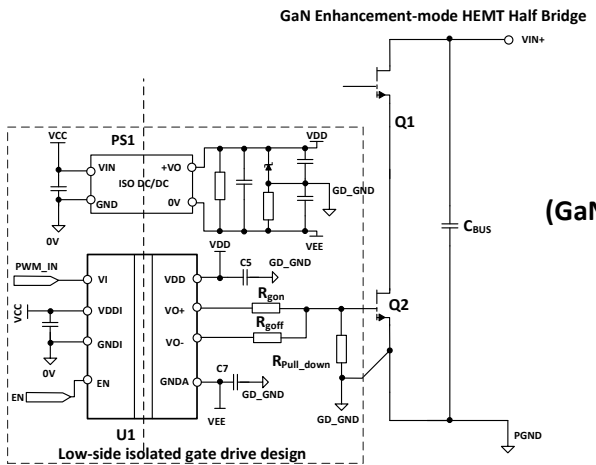


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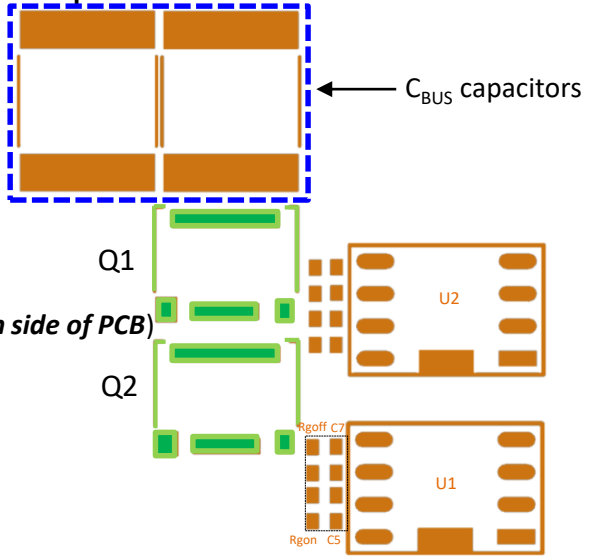
Step 2.2: Gate Driver Circuit Loop (Top-side cooling)

Example: Isolated gate driver circuit w/ single GaN HEMT

- Locate drivers close to the gate
- Use/create kelvin source for driver return

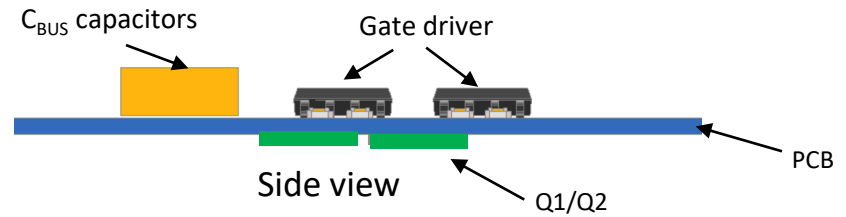


Component Placement



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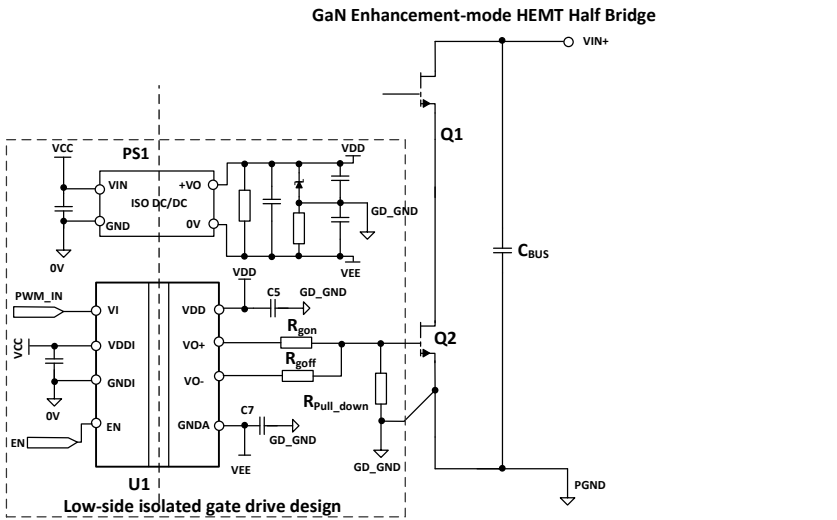
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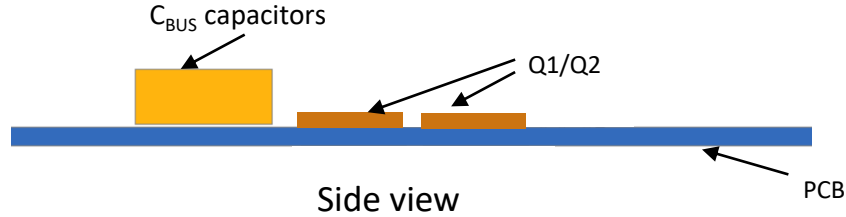
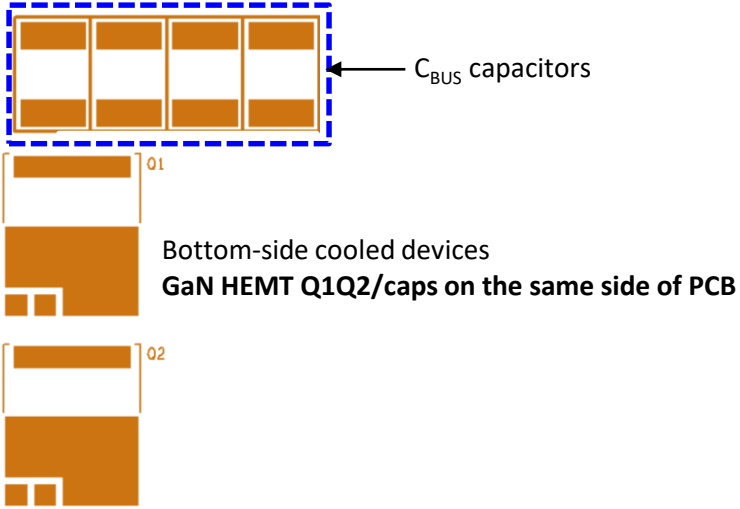
Step 2.1: Power commutation loops (Bottom-side cooling)

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- Place components as close together as possible



Component Placement

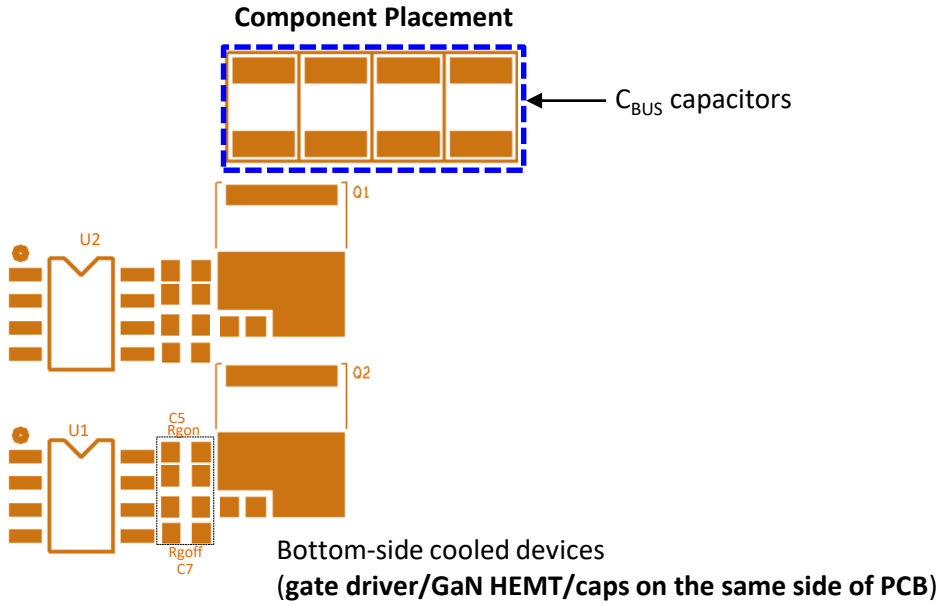
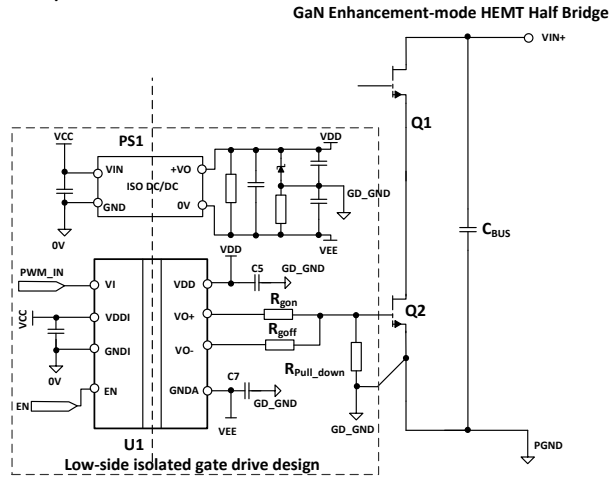


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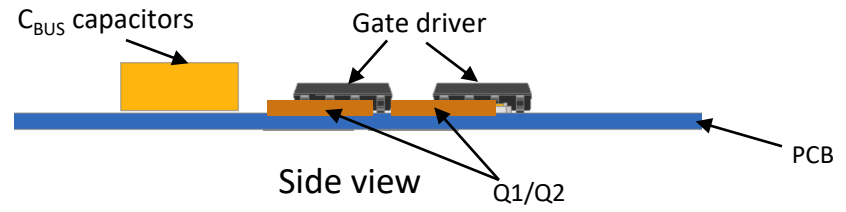
Step 2.2: Gate Driver Circuit Loop (Bottom-side cooling)

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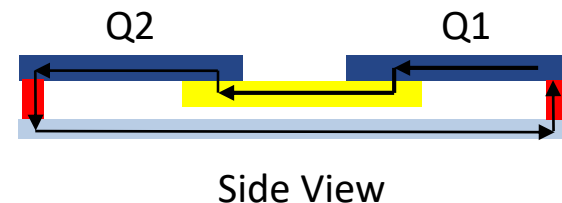
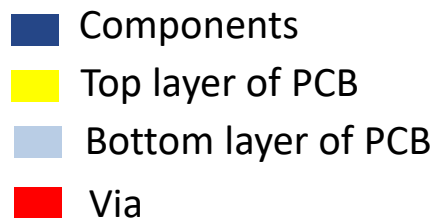
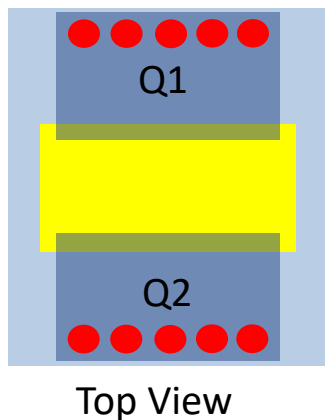
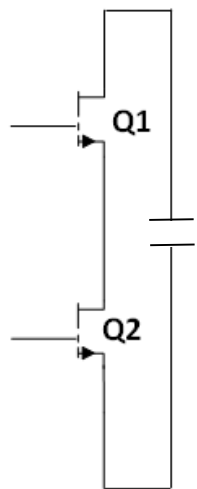
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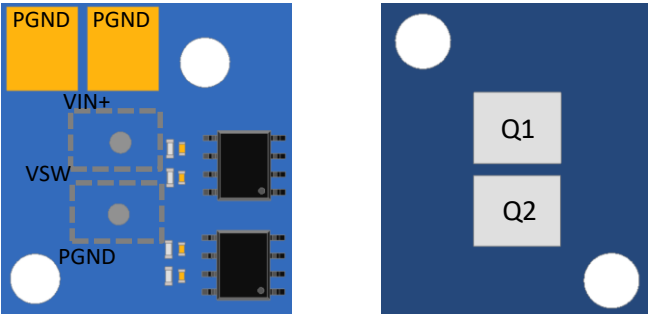
- When two adjacent conductors are located close with opposite current direction, magnetic flux generated by two current flows will cancel each other.
- This magnetic flux canceling effect can lower the parasitic inductance.
- Arrange the layout so that high-frequency current flows in opposite direction on two adjacent PCB layers.



Step 3.2: Connect the components with Flux-cancelling traces

- Connect the components with Flux-cancelling traces, see below example of top-side cooled devices and bottom-side cooled devices.

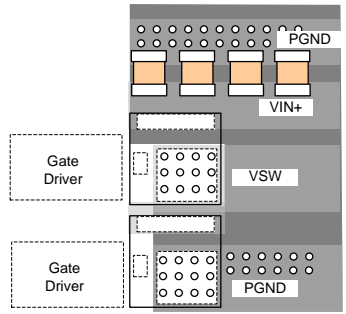
Example: Top-side cooled devices
(GaN HEMT is on the bottom side of PCB)



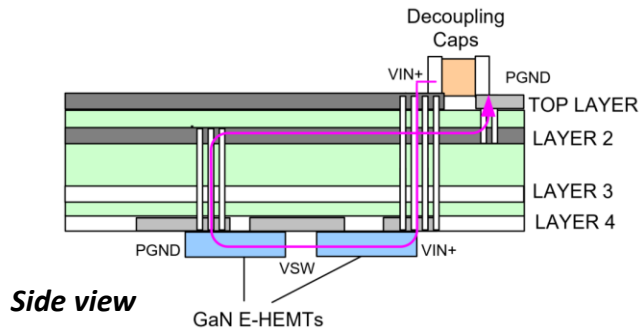
Top view

Bottom view

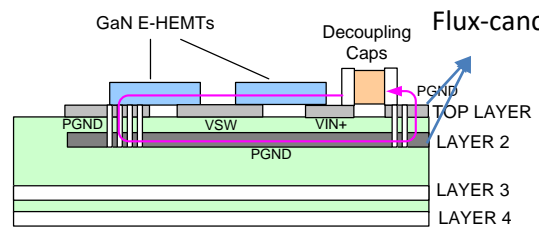
Example: Bottom-side cooled devices
(gate driver/GaN HEMT/caps on the same side of PCB)



Top view



Side view



Side view

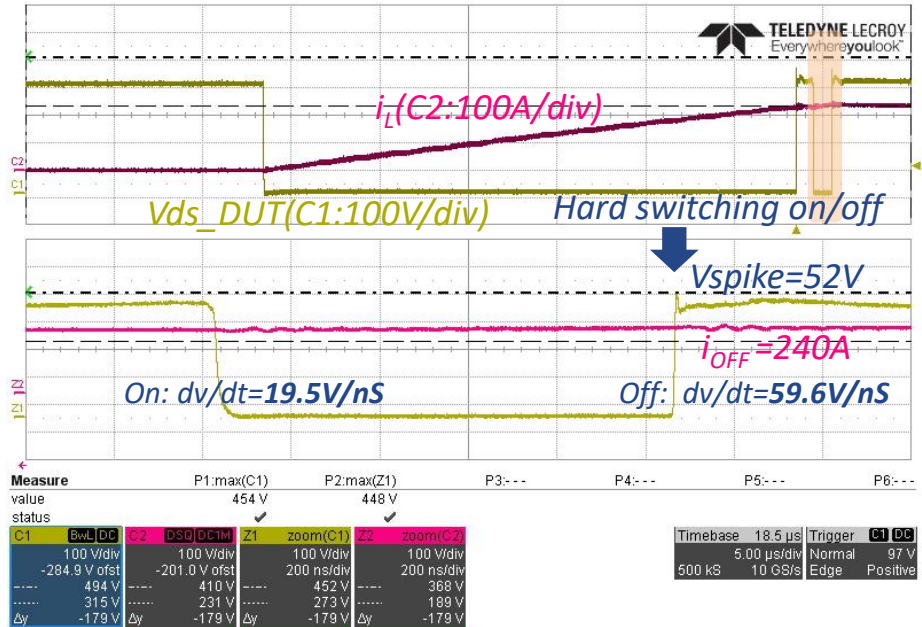
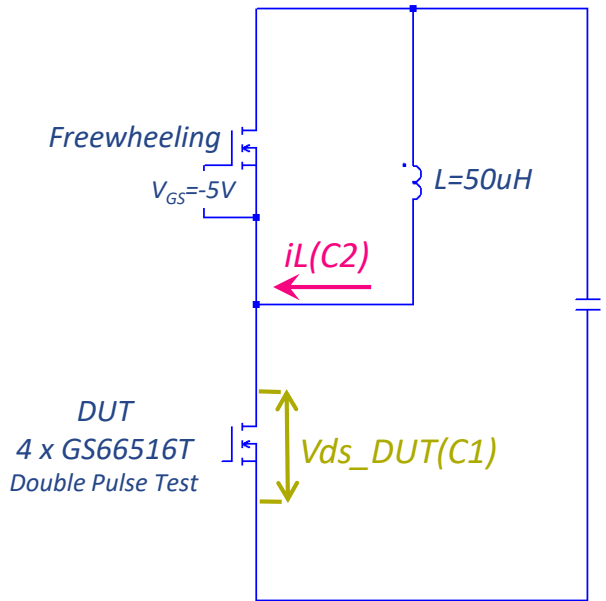
Use layer 2 as ground return (4-layer PCB)

Experimental Example: 400V/240A DPT Hard-switching Test

DUT: 4 x GS66516T in parallel.
 Freewheeling: 4 x GS66516T in parallel

Test conditions

- $V_{BUS} = 400\text{ V}$
- $I_{DS_ON} = 231\text{ A}$
- $I_{DS_OFF} = 240\text{ A}$
- $V_{GS} = +6.8\text{ V}/-5\text{ V}$
- $R_{G_ON} = 4.55\ \Omega$
- $R_{G_OFF} = 1.25\ \Omega$



Measurement Setup: Lecroy WaveSurfer 10M Oscilloscope, HVD3106 Differential Probe(C1), CWT-3LFB mini Rogowski Coil(C2)

- Using good engineering practice for PCB layout in designs where GaN Systems' E-HEMTs are paralleled, current balancing and clean switching can be achieved. Hard switched is possible to full rated current.
- This example demonstrates ~200V V_{DS} margin on a 400V/240A hard-switching test

- Due to faster switching speed of GaN E-HEMTs, good engineering practice for PCB layout techniques are required to minimize parasitic inductance and fully utilize these advanced devices.
- Optimizing the PCB layout is important to achieve the maximum performance capability of GaN based designs. With optimum board layout combined with low GaNPX[®] package inductance, GaN Systems' E-HEMTs exhibit peak switching performance.



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