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System Level Considerations with GaN Power Switching

Preface March 7th, 2018

APEC Industry Session - San Antonio, Texas

System Level Considerations with GaN

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Digest

Gallium Nitride (GaN) transistors have been implemented into many power electronics applications by innovative and mainstream power electronics companies. GaN E-HEMTs (high electron mobility transistors) are used in applications for wireless charging and power transfer, DC motors for appliances, data center power, factory automation, solar, energy storage systems, and electric and autonomous vehicles. GaN enables the significant increase in efficiency that reduces losses, diminishes size, increases power density, prolongs battery life, and reduces bill-of-materials, capital expenditure and operating costs. All desirable outcomes in the mentioned applications. This presentation will demonstrate how the unique characteristics of GaN enable the performance of the HEMTs to produce the energy, weight, size and system cost reductions.

This presentation delve into the key parameters that affect performance, like gate charge, capacitance, drain-to-source resistance (including dynamic effects) and transconductance. The effects of temperature on these parameters will be discussed.

Topologies with that benefit from GaN E-HEMTs will be analyzed. The topologies to be analyzed include bridgeless totem pole for PFC, LLC half-bridges, phase-shifted full bridge. Very low dead times and fast switching are being enabled by GaN's low latency, fast switching, high frequency, ease of driving and high current capability. The low dead times further enable innovation in control techniques, new topologies and magnetics.

Thermal characteristics of GaN and its packaging will be demonstrated for enhancing system level thermals and packaging effectiveness.

GaN qualification, reliability and standards have been popular topics in the power electronics industry. A discussion on the topic will demonstrate the how the wide bandgap transistor industry is coming together create standards and guidelines for test methods, reliability, qualification procedures, and datasheet parametrics for GaN based power conversion devices.

The presentation is aimed at intermediate power electronic design engineers and system engineers. The benefits of GaN transistors will also be of interest to power electronics technical marketing, business development, quality, reliability and component engineering professionals.

Biographies

Peter Di Maso is director of product line management at GaN Systems and is responsible for creating and executing a sustainable portfolio of GaN power products. Peter has more than 20 years' experience in the power electronics industry. Peter's background includes strategic product marketing at Texas Instruments, where he helped establish TI's LED lighting product line. Peter also has gained experience from, and contributed to the success of leading power management semiconductor companies Maxim Integrated Products, Analog Devices and Allegro Microsystems.

Peter Di Maso has a Bachelor of Engineering degree (Electrical) from Concordia University in Montreal, QC, Canada and a Masters of Business Administration from Southern New Hampshire University in Manchester, NH, USA

Di Chen received his M.Sc in power electronics from Univ. of British Columbia in 2009 with research interest in power electronics design for renewable energy hybrid power systems. He has 8 years of power electronic system design experience.

In 2011, Di joined Honeywell and was responsible for power inverter design for industrial process control. He joined GaN Systems in 2014 where he has been working on customer application support and reference designs for next generation Gallium Nitride (GaN) HEMT based power systems.

Di Chen is in responsible for global application support, manages the head office applications and worldwide FAE team. He is an IEEE member and registered Professional Engineer in Ontario Canada.

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Topics - System Level Considerations with

GaN E-HEMT Characteristics

- Similarities and Differences to MOSFETs

Low Loss Switching and Conduction in GaN

GaN E-HEMTs Key Parameters - Reducing System Losses and Parallel Operation

- Gate Charge, On Resistance, Threshold Voltage and Transconductance

Topologies and Applications Enabled by GaN

Thermal Capabilities Providing High Density Power Conversion

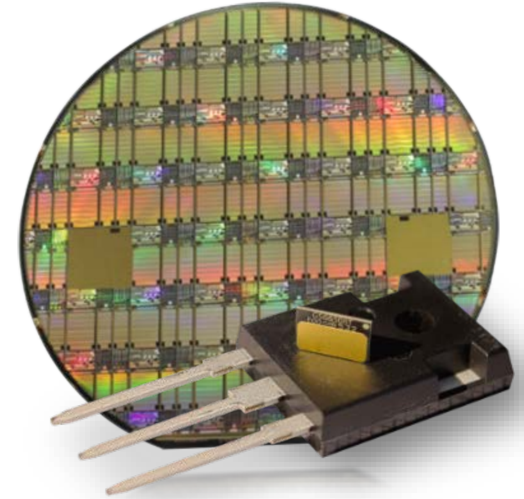
GaN E-HEMT Industry Coming Together to Establish Guidelines & Standards

Summary

GaN Systems - Company Overview

Market leader for gallium nitride (GaN) power transistors

- Enhancement mode devices
- 100V & 650V devices.
- High current devices (100V to 120A, 650V to 120A)
- Industry's most robust gate drive with +10/-20V range
- GaN*PX*® embedded power package for performance



GaN*PX*® vs TO-247

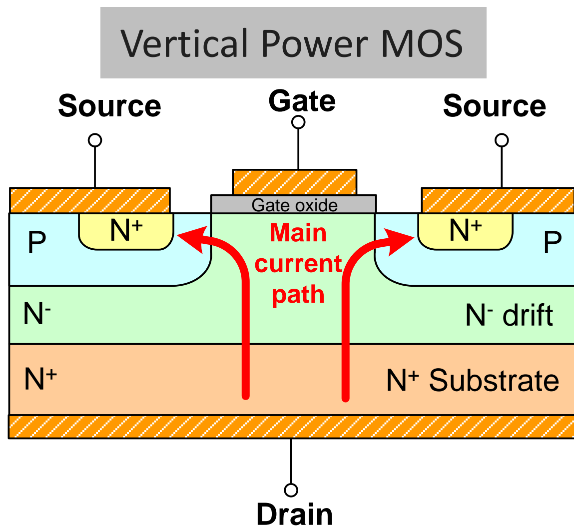
Global company with decades of GaN experience

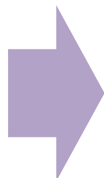
- Founded 2008
- Shipping product since 2014
- HQ and R&D in Ottawa, Canada
- Global Sales & Applications support
- World-class fabless manufacturing and advanced packaging

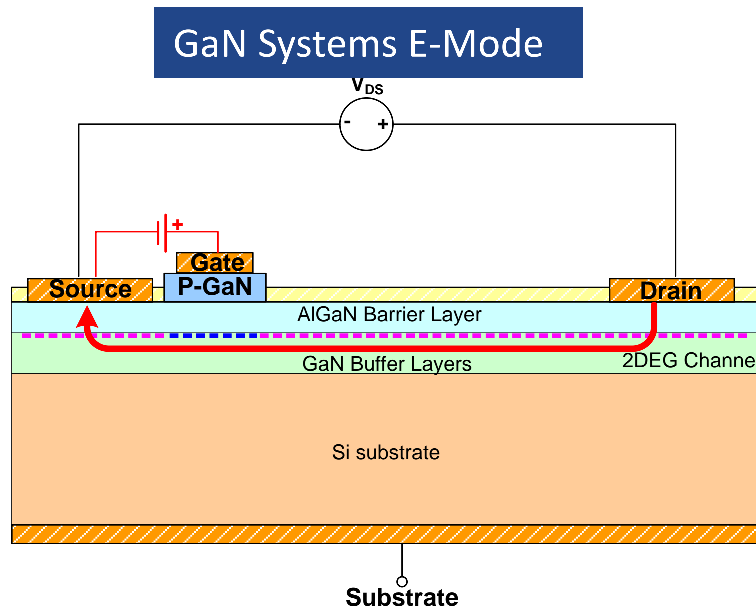
GaN E-HEMT Fundamentals

GaN High Electron Mobility Transistor (HEMT)

- Epi-growth of GaN on standard high volume silicon wafer,
- 2-Dimensional Electron Gas (2DEG) is formed at the hetero-interface between GaN and AlGaN
- 2DEG has very high charge density and mobility: very low $R_{DS(on)}$ and high speed device
- P-type GaN depletes 2DEG channel underneath, a positive gate bias turns on the 2DEG – Normally off e-mode
- Voltage driven like Si MOSFET
- No Gate Oxide: high gate reliability





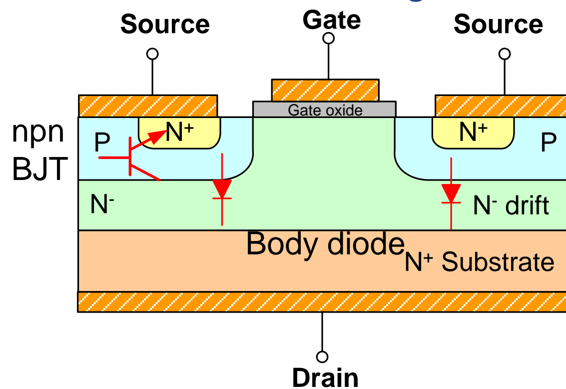


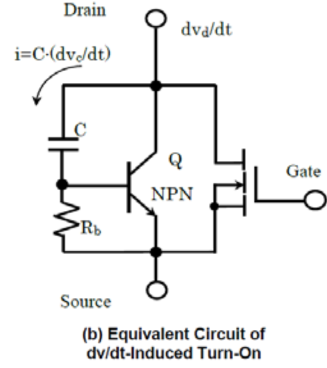
Similar to MOSFET with much faster, more efficient switching

GaN vs Si Comparison

Si MOSFET

- Parasitic BJT and body diode
- dv/dt Failure
- High reverse recovery charge Q_{RR}
- Not ideal for half bridge hard-switching





(b) Equivalent Circuit of dv/dt-Induced Turn-On

MOSFET dv/dt Limit

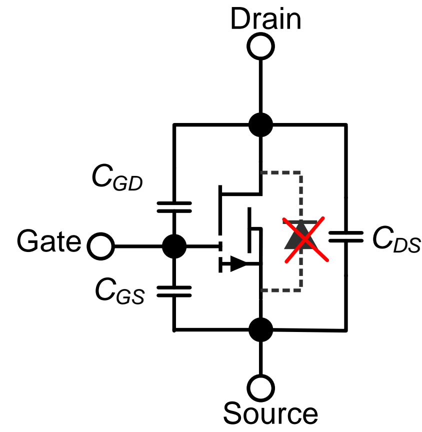
MOSFET dv/dt ruggedness	dv/dt	-	-	80	V/ns

MOSFET Body diode Q_{RR}

Reverse recovery charge	Q_{rr}	-	10	-	µC

GaN E-HEMT

- No parasitic BJT and body diode
- High dv/dt ruggedness
- Zero reverse recovery
- 2DEG can conduct in reverse, no need for anti-parallel diode
- Fit for half bridge hard & soft switching

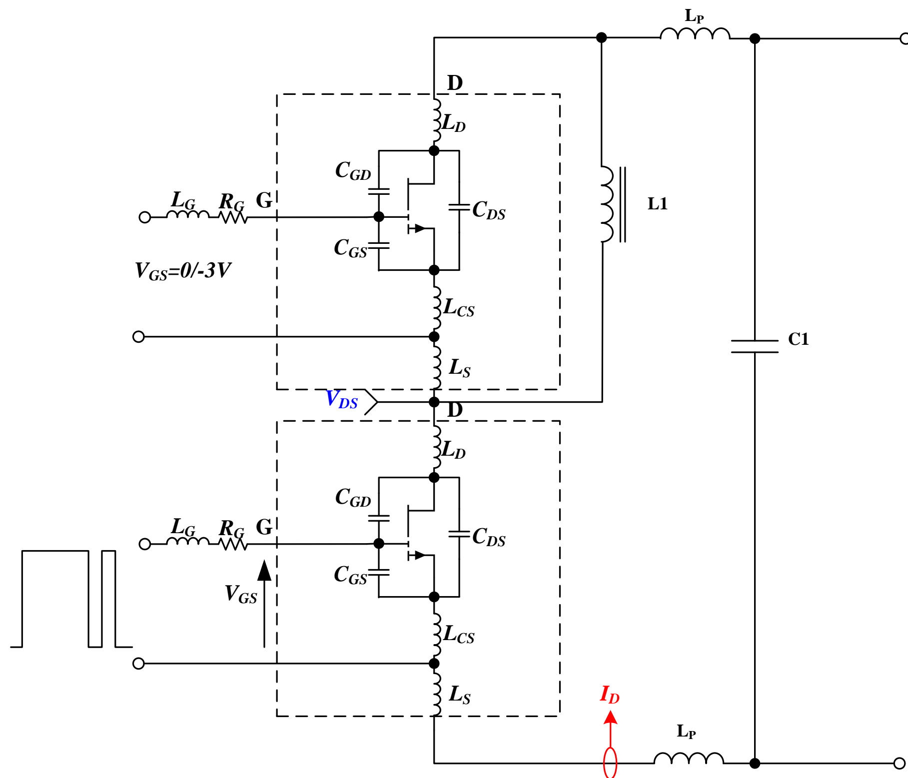


GaN E-HEMTs ruggedness, no reverse recovery and reverse conduction provide implementation advantages

GaN Switching – Circuit Board, Package and

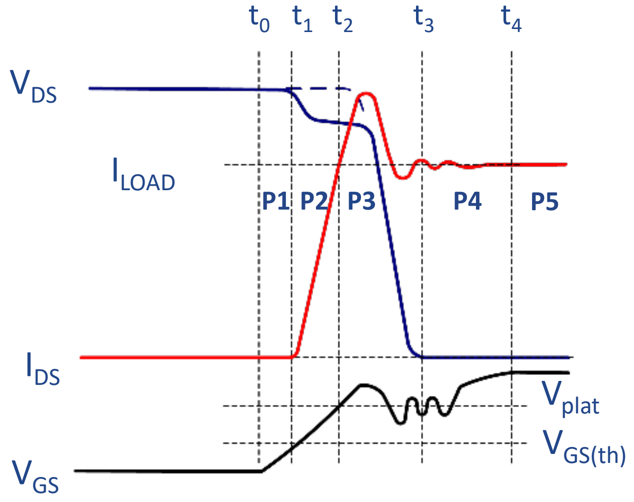
- Circuit model used for explanation
  - L_G – gate loop parasitic inductance
  - L_D – drain parasitic inductance
  - L_S – source parasitic inductance
  - L_{CS} – common parasitic inductance
  - L_P – power loop parasitic inductance
  - C_{GS} = gate to source capacitance
  - C_{GD} – gate to drain capacitance
  - C_{DS} – drain to source capacitance

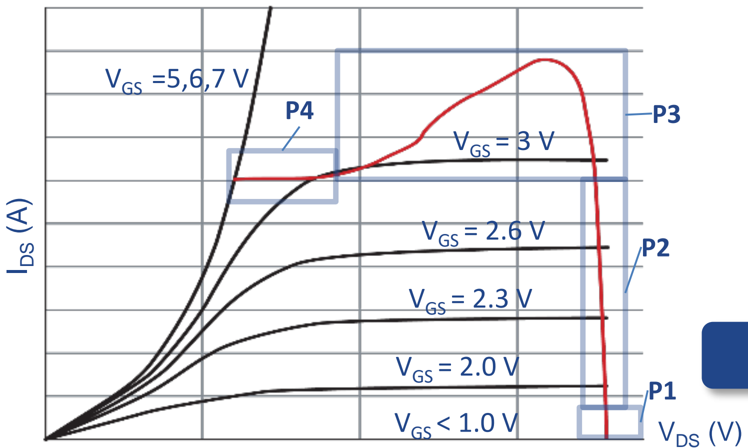
$C_{ISS} = C_{GS} + C_{GD}$
$C_{RSS} = C_{GD}$
$C_{OSS} = C_{DS} + C_{GD}$



Consideration of key parameters for GaN

Turn On and Conduction Processes



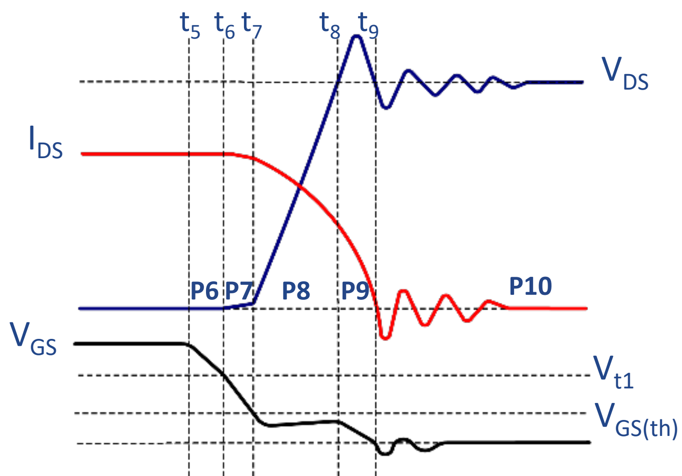


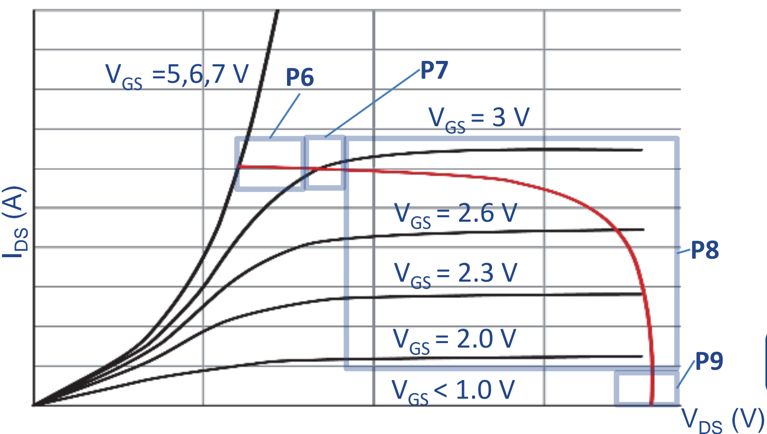
Low Side Switch Turn On		
Period	Time	Summary
P1 ($t_0 \rightarrow t_1$)	Delay Period	Small C_{ISS} of GaN E-HEMT results in a low gate driver loss and short delay time.
P2 ($t_1 \rightarrow t_2$)	di/dt (V*I loss) region	Low C_{ISS} and parasitic inductance of GaN*PX*™(L_G, L_{CS}) allows faster di/dt and lower switching loss with GaN E-HEMT
P3 ($t_2 \rightarrow t_3$)	dv/dt (Miller Plateau)	Low C_{RSS}, C_{OSS} and no Q_{RR} are the key to fast turn-on dv/dt and low switching loss of GaN E-HEMT
P4 ($t_3 \rightarrow t_4$)	Stabilization	Low inductance of GaN*PX*™ package reduces the gate overshoot
P5 ($t_4 \rightarrow t_5$)	Conduction	Effective $R_{DS(on)} * I_D^2$

An Experimental Comparison of GaN E-HEMTs versus SiC MOSFETs over Different Operating Temperatures by Jianchun Xu, download here: https://gansystems.com/design-center/papers/

Input, Output and Reverse Capacitance Deliver low-loss turn on

Turn Off Process





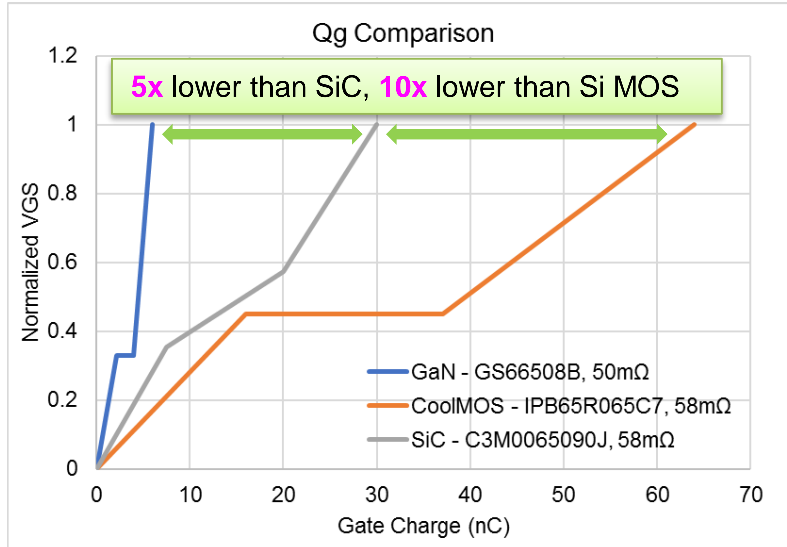
Low-Side Switch Turn Off		
Period	**Time**	**Summary**
P6 ($t_5 \rightarrow t_6$)	Delay Period	Small C_{ISS} of GaN E-HEMT results in short delay and fast turn-off
P7 ($t_6 \rightarrow t_7$)	2DEG Loss Period	Due to the ultra-fast transition of GaN E-HEMT, switching loss at turn-off is very small
P8 ($t_7 \rightarrow t_8$)	dv/dt (C_{OSS} charging)	Fast transition of GaN E-HEMT causes 2DEG to open as V_{DS} rises resulting in no loss in dv/dt (Miller plateau) period
P9 ($t_8 \rightarrow t_9$)	di/dt (overshoot)	Low parasitic inductance and Kelvin source sense of GaNPX™ package minimizes the spike and ringing.
P10 ($t_9 \rightarrow t_1$)	Off time	

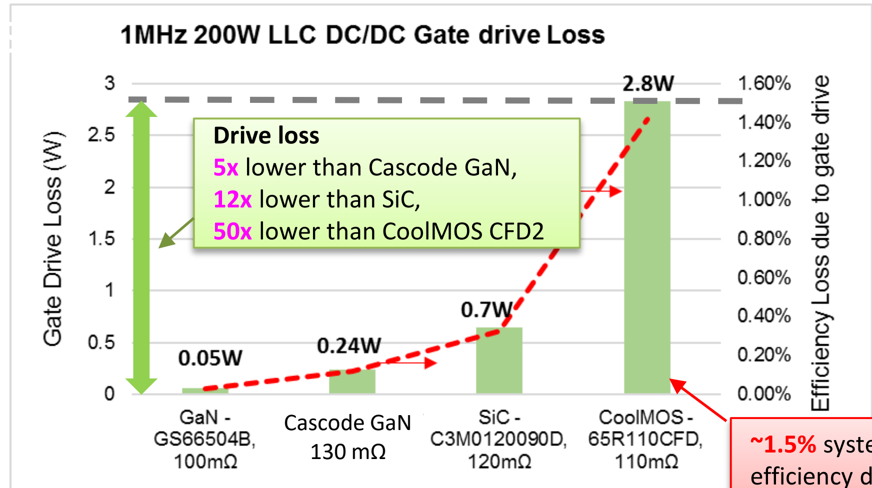
An Experimental Comparison of GaN E-HEMTs versus SiC MOSFETs over Different Operating Temperatures by Jianchun Xu, download here: https://gansystems.com/design-center/papers/

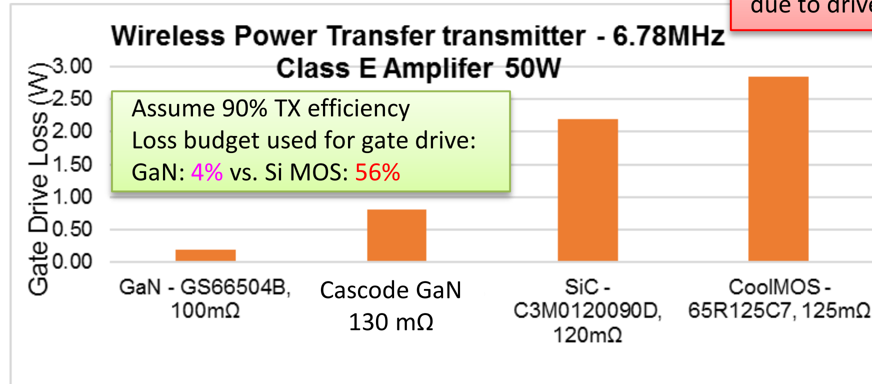
Turn off switching loss greatly reduced compared to MOSFET

GaN Performance – Ultralow Gate Drive

- 5-10x smaller than equivalent Si MOSFET
- Up to 50x lower gate drive loss at MHz switching







Low Q_G key to efficient high f_{sw} operation

Paralleling advantages of GaN E-HEMTs

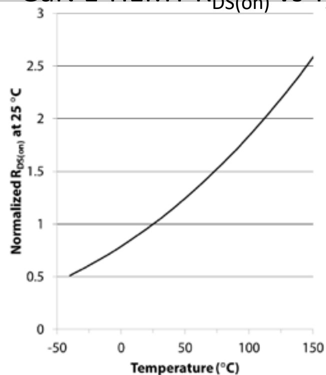
On Resistance Temperature Dependency

- GaN E-HEMT has positive temperature co-efficient $R_{DS(on)}$
- Helps the current sharing in parallel operation

Threshold Voltage Temperature Dependency

- GaN E-HEMT has stable gate threshold over the temperature range
- Si/SiC MOSFET $V_{GS(th)}$ decreases with temperature:
  - Hotter drive turn-on earlier potential runaway

GaN E-HEMT $R_{DS(on)}$ vs T_J



SiC $R_{DS(on)}$ vs T_J

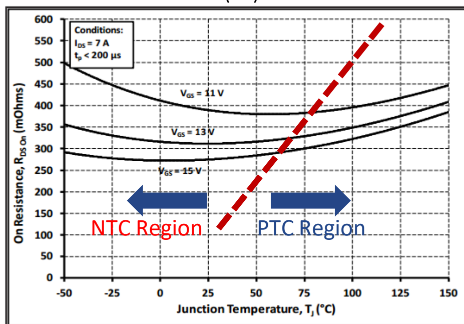
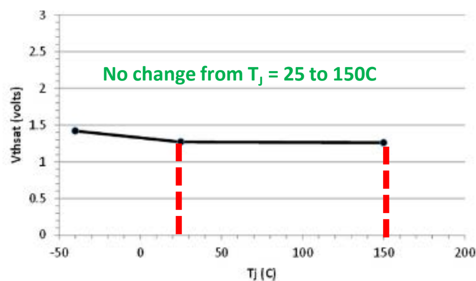
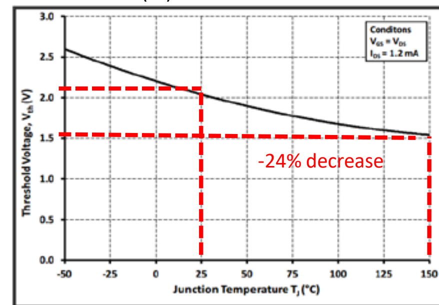


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

GaN E-HEMT $V_{GS(th)}$ over T_J range



SiC $V_{GS(th)}$ decreases with T_J

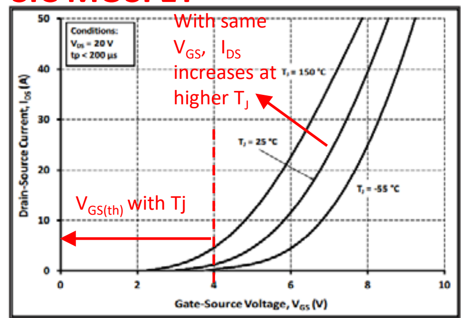


Positive TC for $R_{DS(on)}$ and stable $V_{GS(th)}$ eliminates current mismatch and thermal runaway

Paralleling advantage - Trans-conductance, g_m vs T_J

- GaN E-HEMT Trans-conductance g_m decreases with temperature, good for paralleling

SiC MOSFET



SiC: $V_{GS(th)}$ drops and g_m increases:

- Hotter device has higher switching current -> higher switching loss
- Positive feedback, potential thermal runaway if not designed properly

GaN HEMT

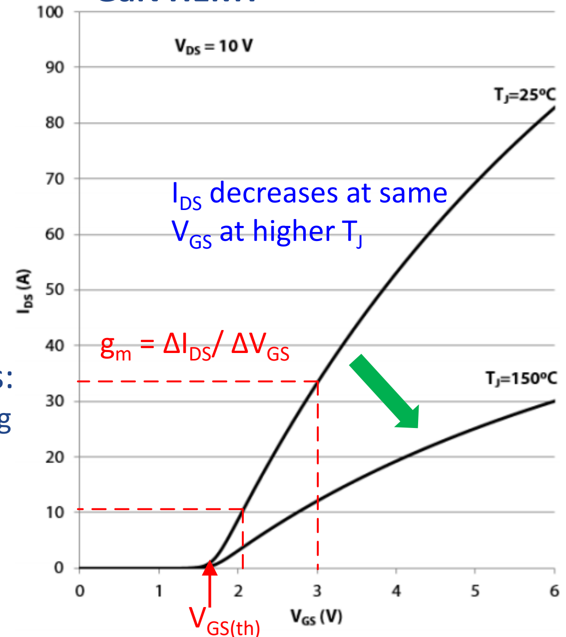
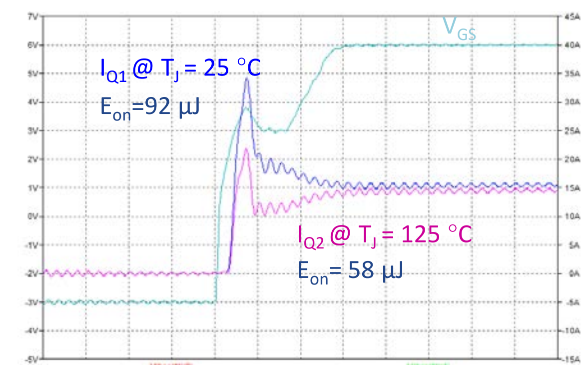


Figure 10 : Typical I_{DS} vs. V_{GS}

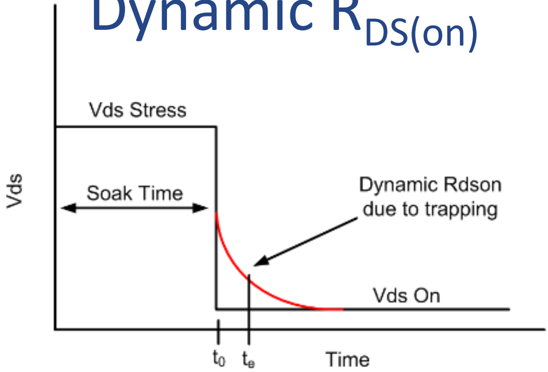
- Negative feedback for self balancing in parallel:
- T_J ↗ - g_m ↘ - $I_{D@switching}$ ↘ - E_{on} ↘ - T_J ↘

2x GS66508T paralleled 400V/30A turn-on waveforms with different T_J



Dynamic Current Sharing and Self Balancing achieved with GaN g_M and $V_{GS(th)}$ characteristics

Dynamic $R_{DS(on)}$



Factors Affecting Dyn $R_{DS(on)}$

- Bias Voltage
- Bias time
- Junction Temperature
- Switching Frequency
- Duty Cycle

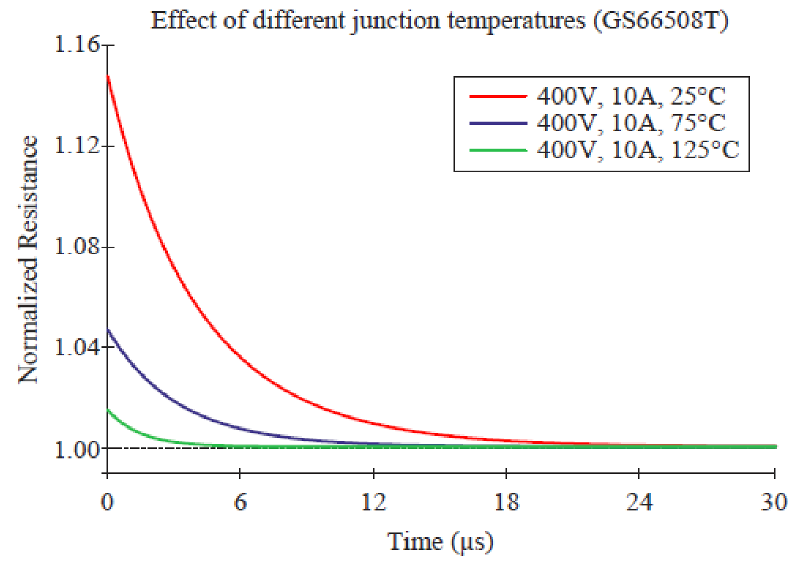


Fig. 14. Normalized R_{dyn} of GS66508T for different junction temperatures

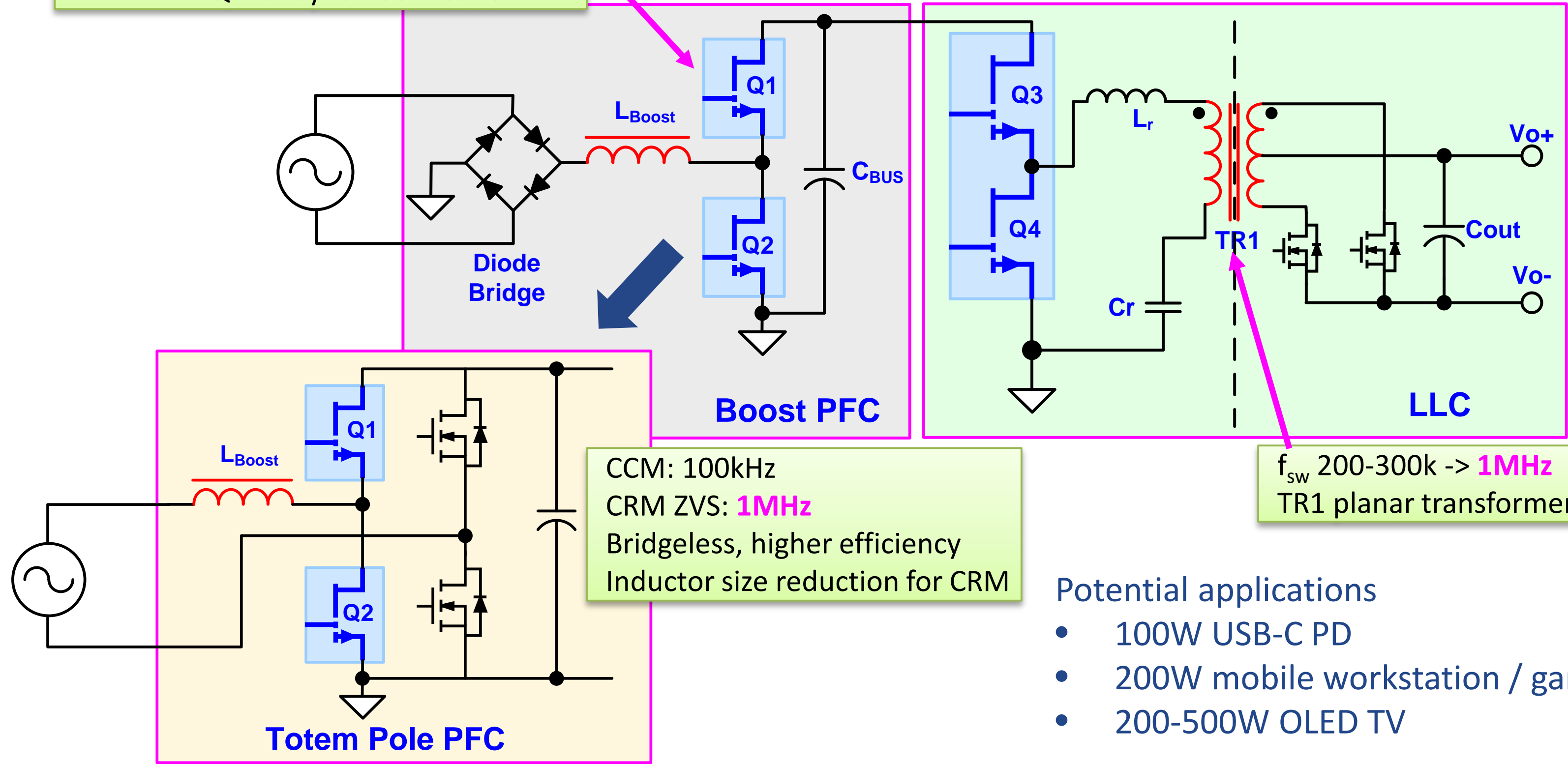
Oliveira, E., Nöding, C., Zacharias, P., (May, 2017) Impact of Dynamic On-Resistance of High Voltage GaN Switches on the Overall Conduction Losses, ISBN 978-3-8007-4424-4

Dynamic $R_{DS(on)}$ affects are negligible in steady state operation

GaN Application – AC/DC Adapter

>75W AC/DC: PFC+LLC

- f_{sw} 100k -> **200kHz**
- Reduces L_{boost} size
- D1 -> Q1 for sync. rectification



CCM: 100kHz
CRM ZVS: **1MHz**
Bridgeless, higher efficiency
Inductor size reduction for CRM

f_{sw} 200-300k -> **1MHz**
TR1 planar transformer reduce height

Potential applications

- 100W USB-C PD
- 200W mobile workstation / gaming laptop
- 200-500W OLED TV

GaN enhances PFC and LLC and enables BTP PFC

200W high density Adapter (PFC+LLC)

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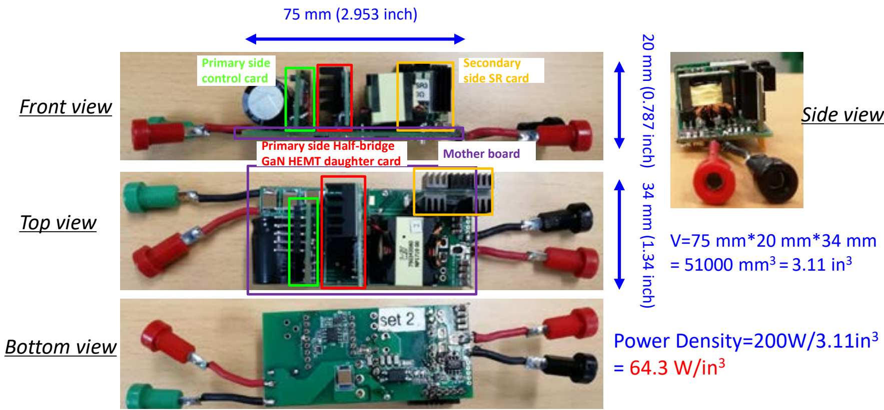
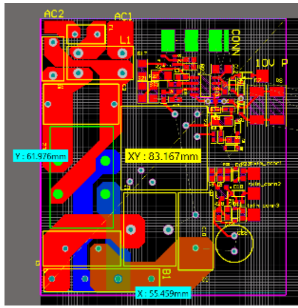
LLC DC/DC stage prototype

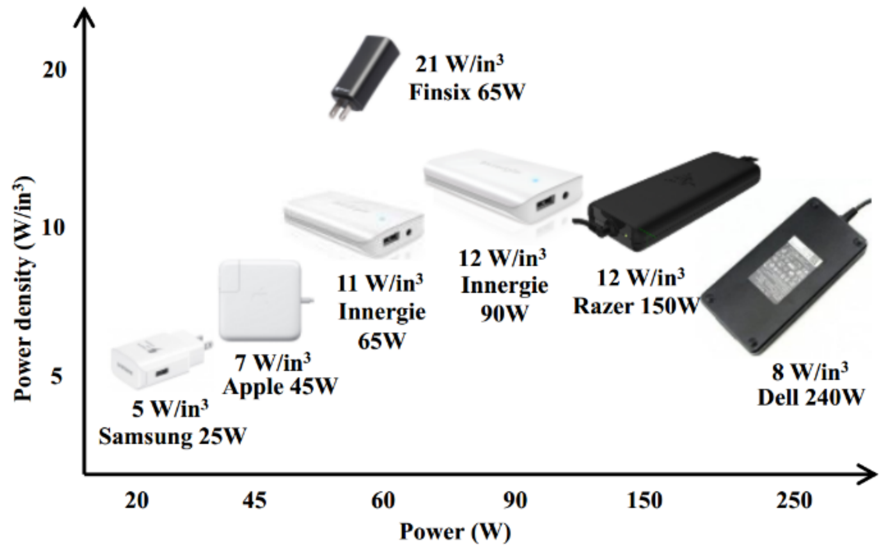


Power Density=200W/3.11in^3
= 64.3 W/in^3

PFC stage board design (4.2 in^3)



- 2-3x smaller size than existing adapter on market
- Efficiency target: 93% total, 96% LLC
- Overall power density (target): **27.36 W/in^3**



Achieves Highest Power Density

Totem Pole PFC: Enabled by GaN

The Value of GaN

- No parasitic BJT and Body Diode
- **Zero** Reverse Recovery
- Reverse conduction, anti-Parallel Diode not required

Smaller Size

- Higher frequency → Smaller filters
- Better topology → Fewer parts
- Lower loss → Smaller heatsink

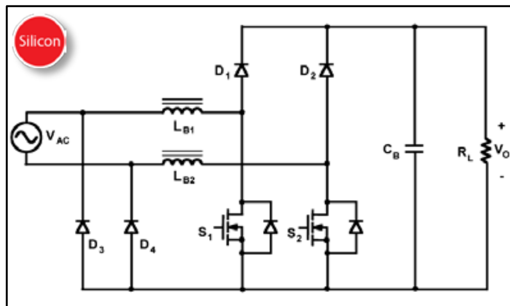
Better Efficiency

- Increases from 97.5% to 99%

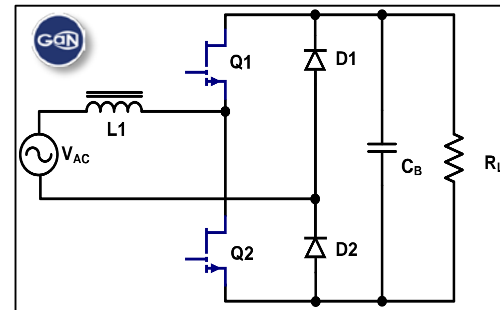
Lower System Cost

- Smaller EMI filter → less expensive
- Smaller heatsink → less expensive

Semi-bridgeless PFC – Si MOSFET

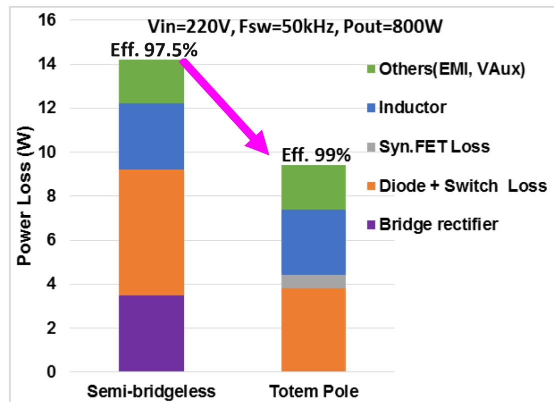


Totem Pole PFC - GaN

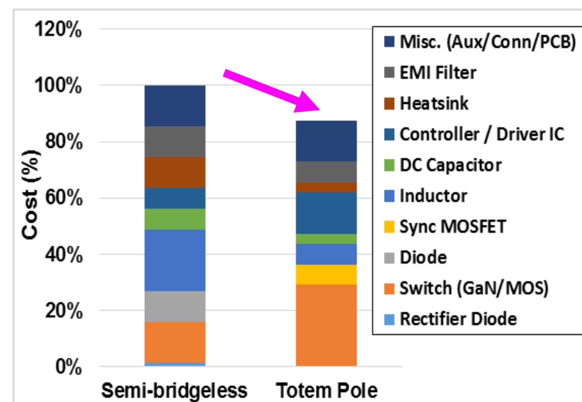


Part count reduced by 33%

PFC Loss Breakdown → 15% lower

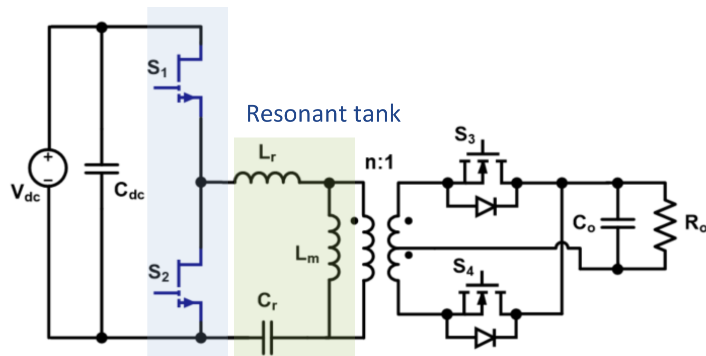


BOM Cost Improvement → 15% lower



GaN makes smaller, more efficient, lower cost PFC solutions possible

LLC DC/DC Converter – GaN Based Design

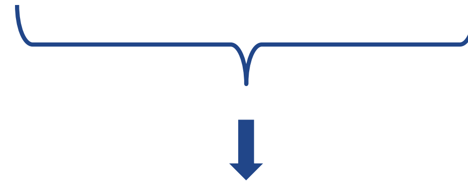


GaN-based half-bridge LLC converter

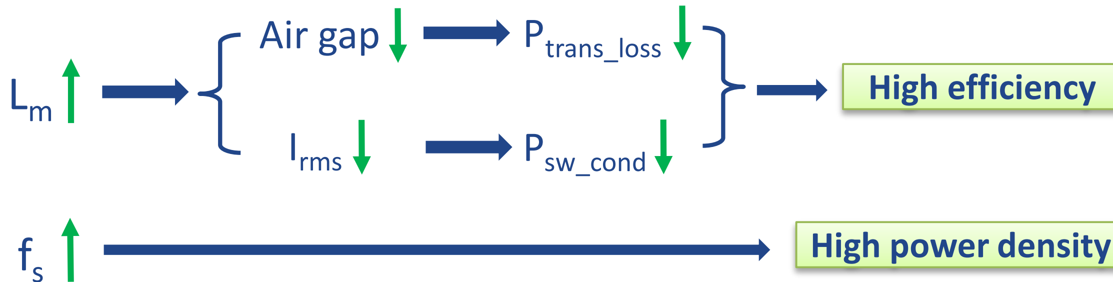
The ZVS constraints of LLC converter

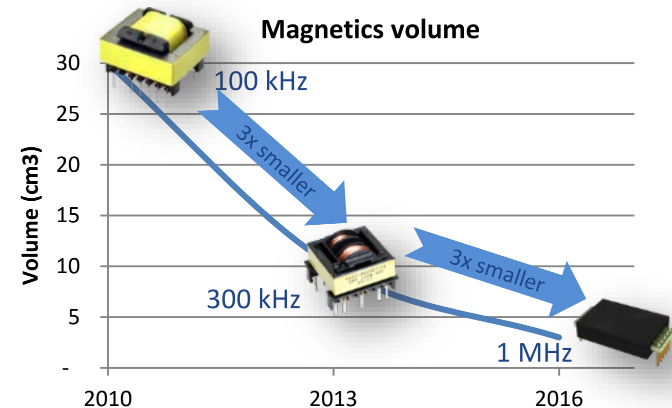
Sufficient deadtime

Sufficient inductive energy from L_m



A smaller C_{oss} leads to:

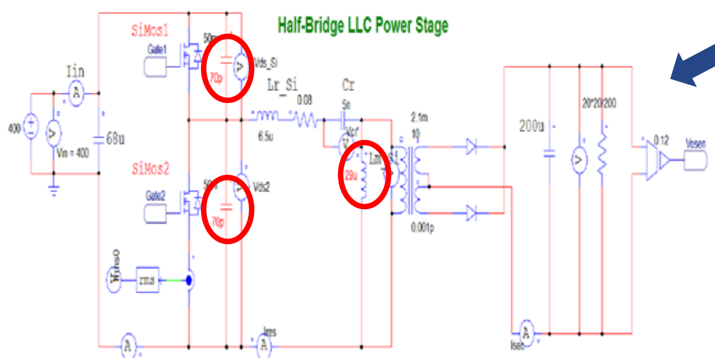




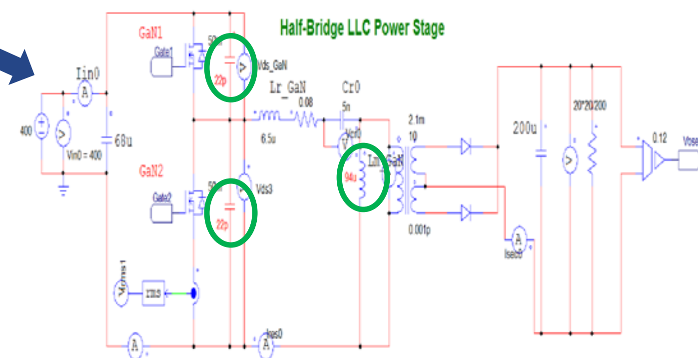
Better switching characteristics of GaN improve LLC efficiency and size

GaN-Based LLC DC/DC Converter

Simulation comparison between Si-based and GaN-based LLC



Converter design specification	
V_{in}	300-400 V
V_o	20 V
I_o	10 A
P_o	200 W
n	10:1:1
F_s	900 kHz
T_{dead}	60 ns



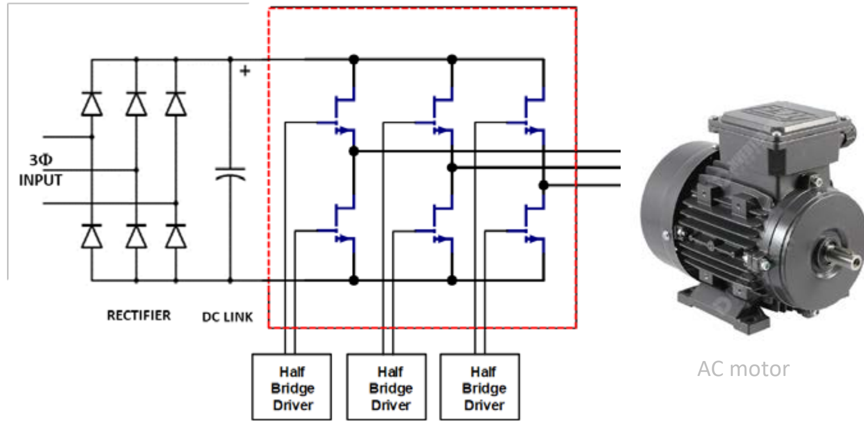
- Same converter requirement is applied to both solutions
- 68% increase on the magnetizing inductance can be achieved with GaN version

Switch parameter comparison	Si MOSFET	GaN HEMT	
	IPA65R190CFD	GS66502B	Unit
V_{DS}	650	650	V
$R_{DS(ON)}$	190	200	mΩ
Q_G	68	1.5	nC
$C_{O\,(ER)}$	70	22	pF
$C_{O\,(TR)}$	336	35	pF

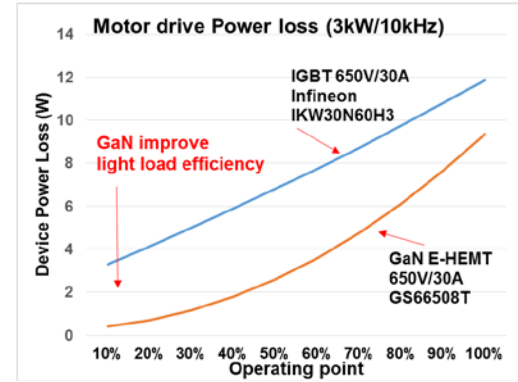
Design parameter comparison	Si MOSFET	GaN HEMT	
	IPA65R190CFD	GS66502B	Unit
L_{m_max}	29	94	µH
I_{rms}	1.3	0.8	A
I_{pk}	2.7	1.9	A
P_{cond}	0.32	0.13	W

GaN based LLC: 60% lower condition losses, 75X lower gate drive loss

Three Phase Half Bridge Inverter for Motor

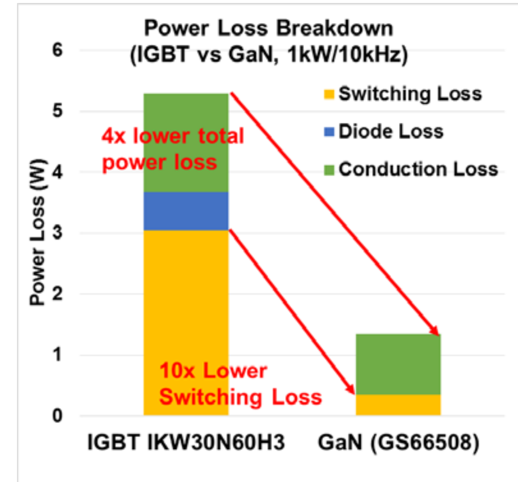


AC motor



The Value of GaN

- **High f_{sw},** → No acoustic noise for quiet operation
  → Smaller and less expensive filtering
  → Sinusoidal output filter for less expensive unshielded cabling, and longer cable lengths
- **Lower Losses**
  → Smaller less expensive heatsinks
  → High Efficiency to meet stringent regulations



GaN Provides Low Frequency, High Current Efficiency and Size

Accelerating the Design Effort - IMS

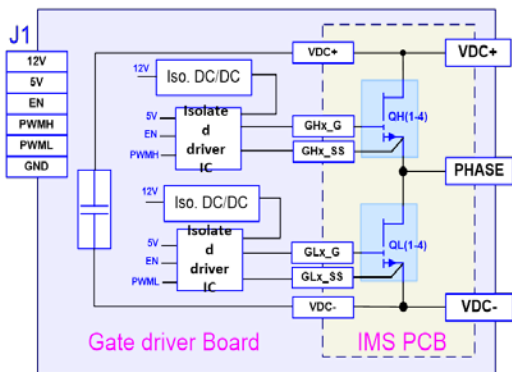
GSP65R25HB-EVB or GSP65R13HB-EVB

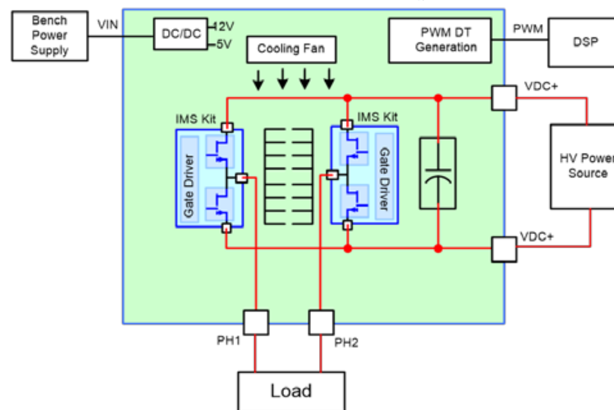
GaN High Power Half Bridge evaluation assembly
(Gate Driver pcb + IMS HB)

IMS Half Bridge Boards
(wo parallel and single transistor)

GSP65MB-EVB

High Power Full Bridge evaluation platform mother board





Uses design concept of higher power GaN intelligent power modules (IPM)

GaNSPEC - GaN Standards for Power Electronic Conversion Devices Working Group

Mission Statement

We seek to create standards and guidelines for Test Methods, Reliability & Qualification Procedures, and Datasheet Parametrics for GaN based power conversion devices

GaN Systems works with industry to standardize GaN information and is founding member of the new JEDEC committee: JC-70 Wide Bandgap Power Electronic Conversion Semiconductors

New JEDEC Committee JC-70

Standards for Wide Bandgap Device Qualification, Test Methods and Datasheet Parameters

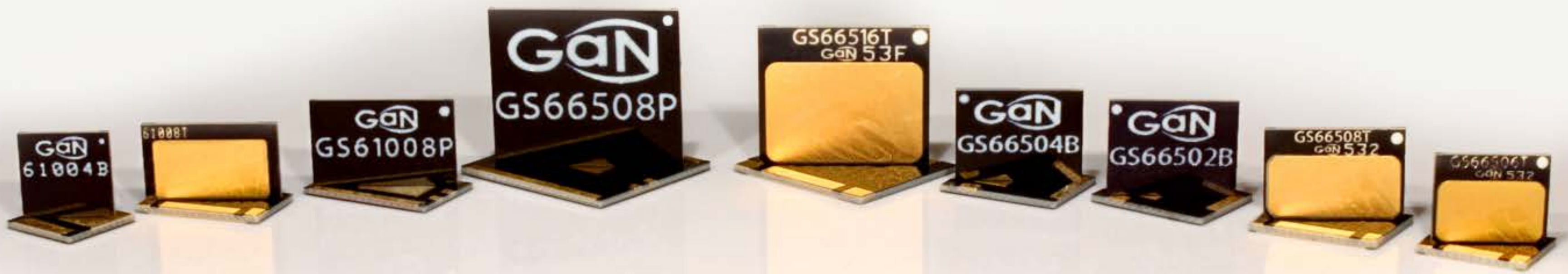
- Members from more than 30 companies: power semiconductor suppliers, users, supply chain representatives.
- Both GaN (JC-70.1) and SiC (JC-70.2) device subcommittees formed
- Interested companies worldwide are welcome to join JEDEC to participate in this important standardization effort.
- Find more information about membership
  - https://www.jedec.org/join-jedec
- Contact Emily Desjardins to learn more (emilyd@jedec.org)
- Get informed! At APEC2018: attend a presentation on JC-70 activity at Industry Session IS16, Thursday March 8 from 8:30 to 11:55.

Summary

- GaN E-HEMTs are mainstream in power electronics design
- Enable topologies and applications
- Reduced losses, weight and volume
- Easy to Use, More Combined Knowledge, Fewer Unknowns
- Lower costs: system, shipping, installation, maintenance and operating costs

Thank You. Please Visit GaN Systems at booth # 1041 for more information and discussion

Thank You



Questions?

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