Opportunities and Design Considerations of GaN HEMTs in ZVS Applications

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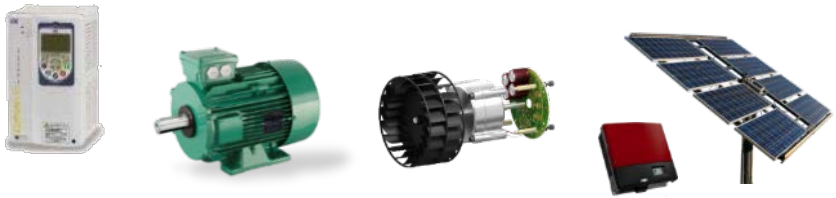
GaN HEMTs today

Consumer

Datacenter

Industrial



Transportation

#1 in GaN

- Highest current; broadest voltages
- Best electrical performance
- Best die & best package
- Most widely used by customers

Shipping since 2014

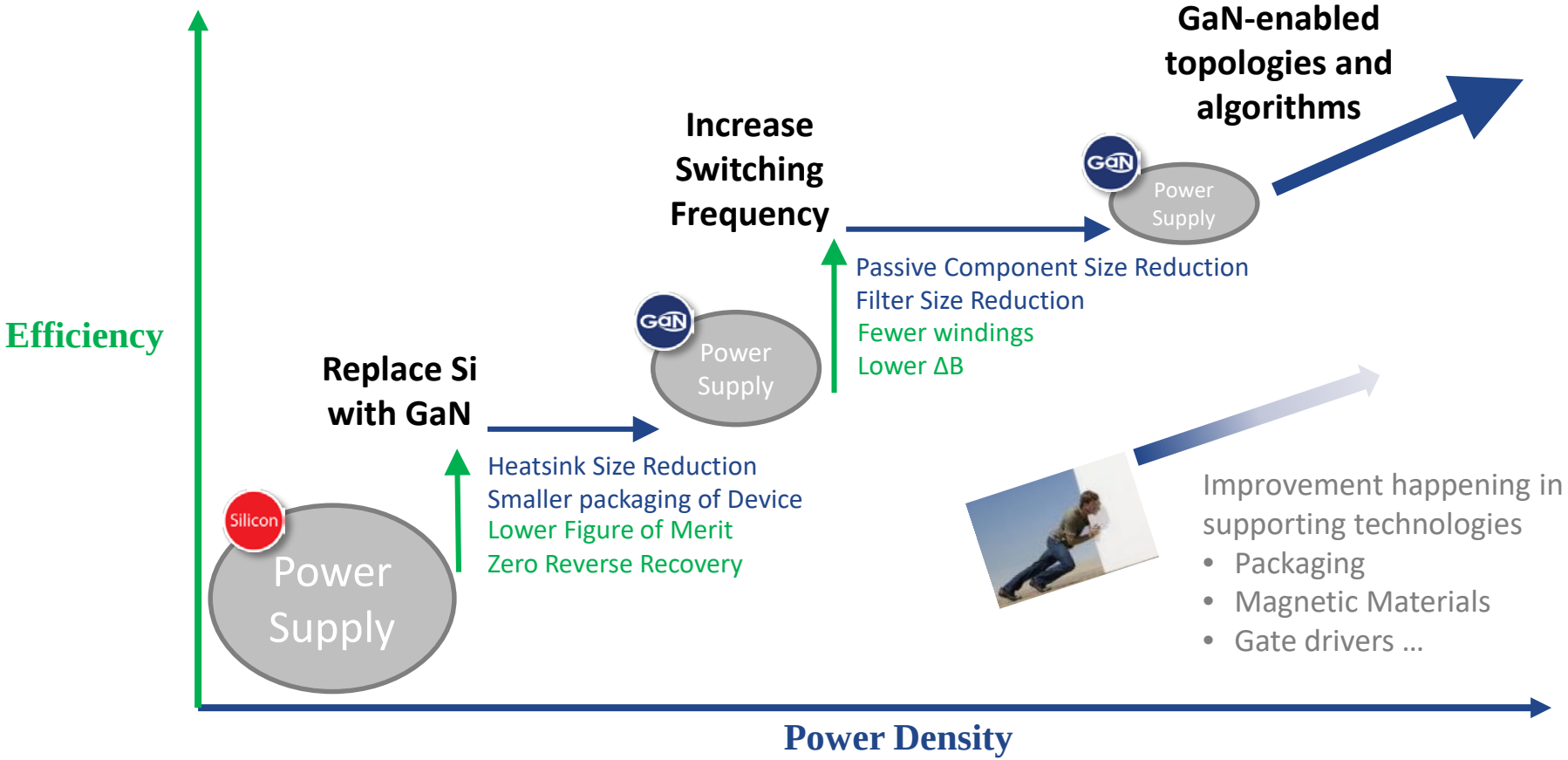
- Offices in 7 countries
- Worldwide disti & direct sales

Customer successes

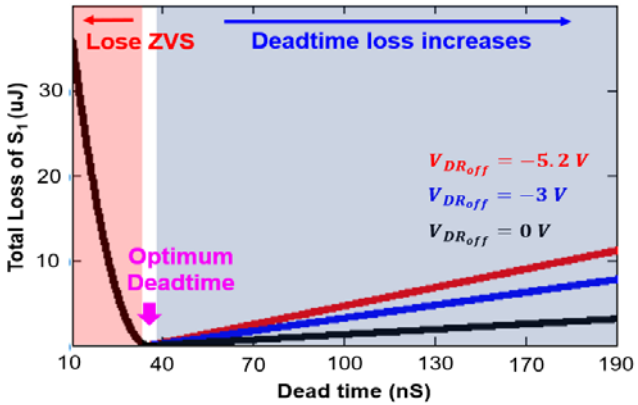
- **Solar Inverter and ESS**
- **Motor Drives**
- Wireless Power and Charging
- AC Adapters
- **Datacenter Server** and Rack Power
- **Automotive Onboard Charger**

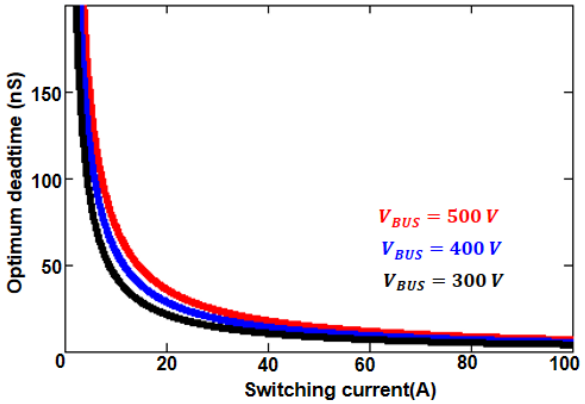
High-power

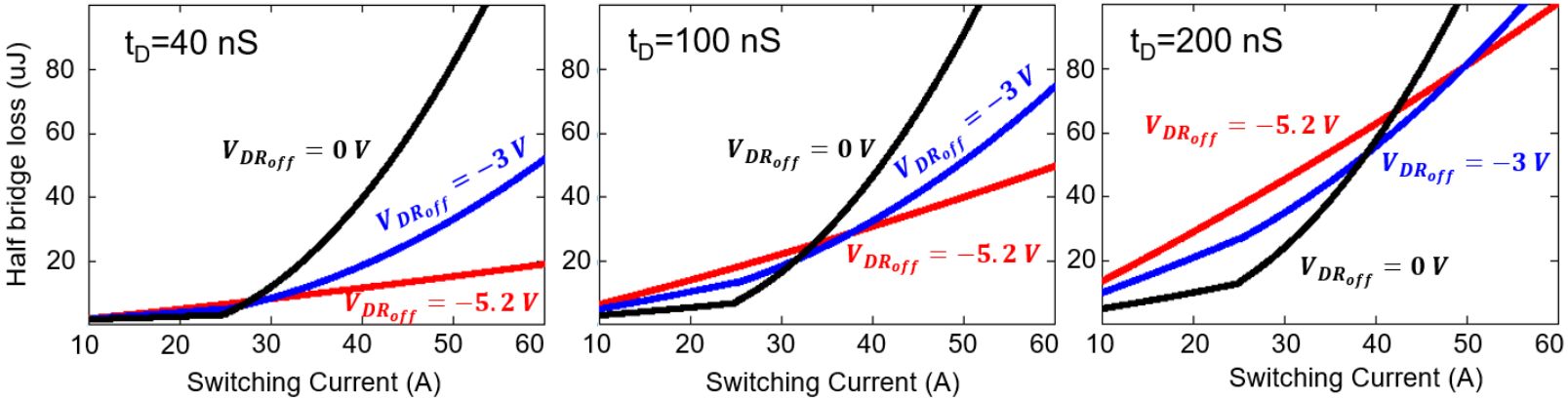
Opportunities with GaN E-HEMTs



Loss Model of GaN HEMTs in ZVS Applications

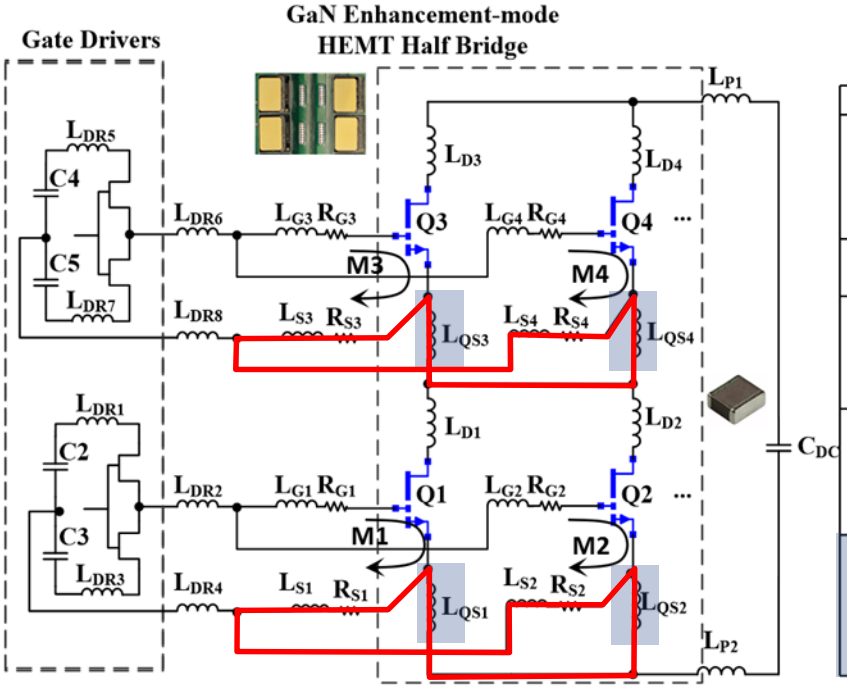






Half-bridge overall loss vs. switching current under different negative turn-off gate voltage V_{DRoff} (a) with deadtime t_D=40 nS, (b) with deadtime t_D=100 nS, (c) with deadtime t_D=200 nS.

Key Parasitics for Paralleling [1]



Effects of Parasitics

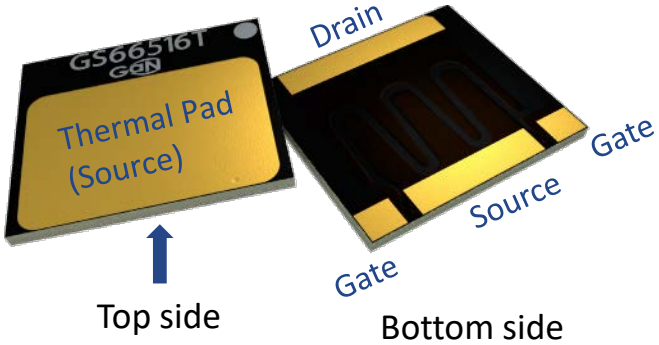
Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} $L_{D1\text{-}4}$	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{S1}-L_{S4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
$L_{QS1\text{-}6}$	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	

Parasitics Optimization is the key to the ultra-high performance of GaN HEMT.

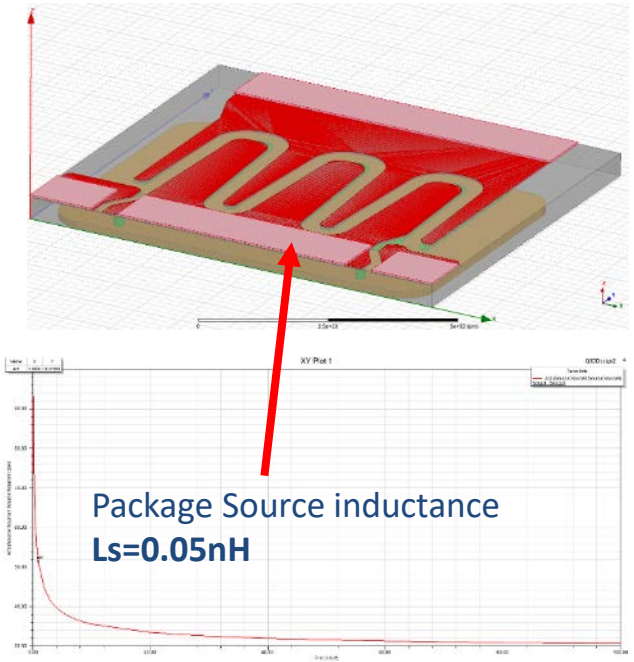
[1] J. L. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW–100kW systems," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 3049-3056. doi: 10.1109/APEC.2017.7931131

Packaging Parasitics of Power Semi-conductors

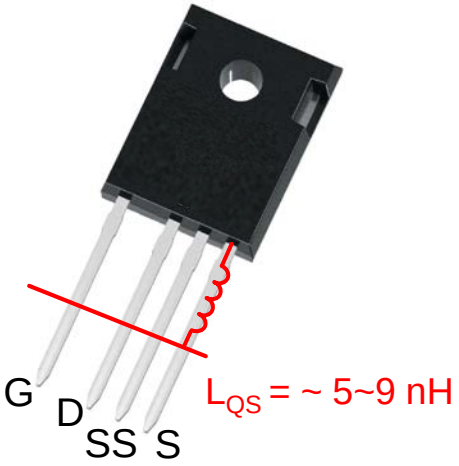
GaN*PX* T Package
GS66516T (650V/25mΩ)



Ansys Q3D 3D modeling of GS66516T

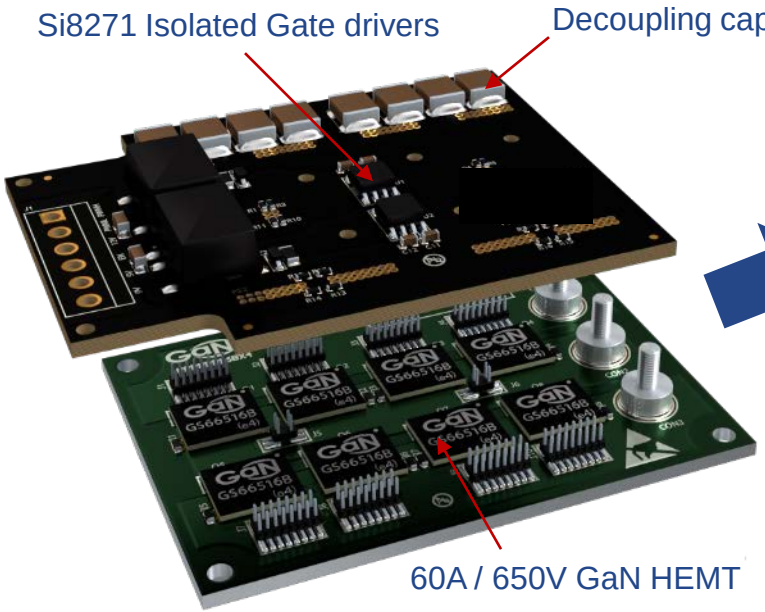


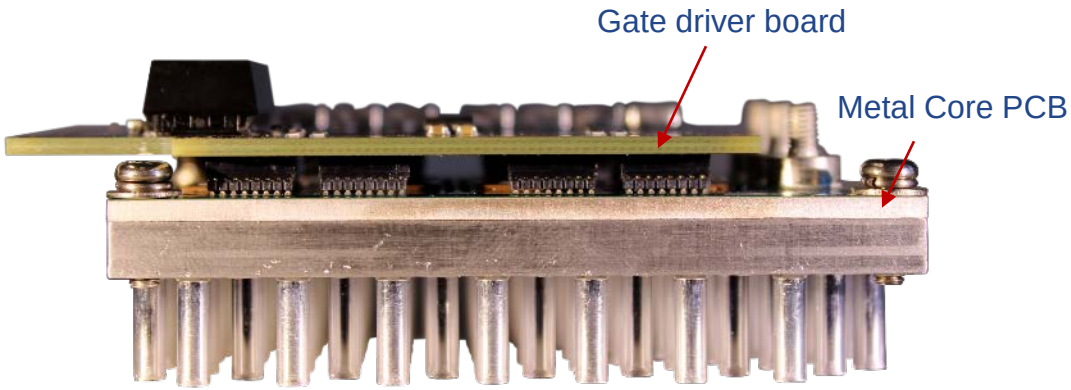
TO-247 Package inductance



GaNPX has ultra-low Ls compared to traditional package.

Reference Design of 240A/650V GaN Module



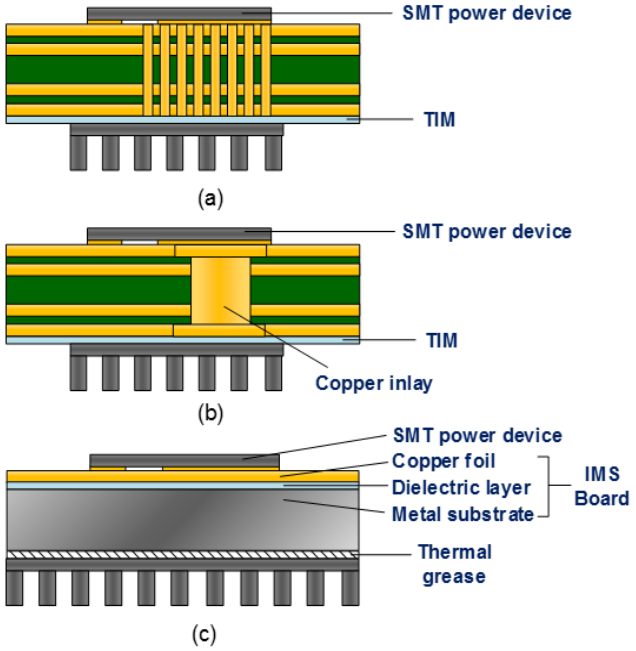


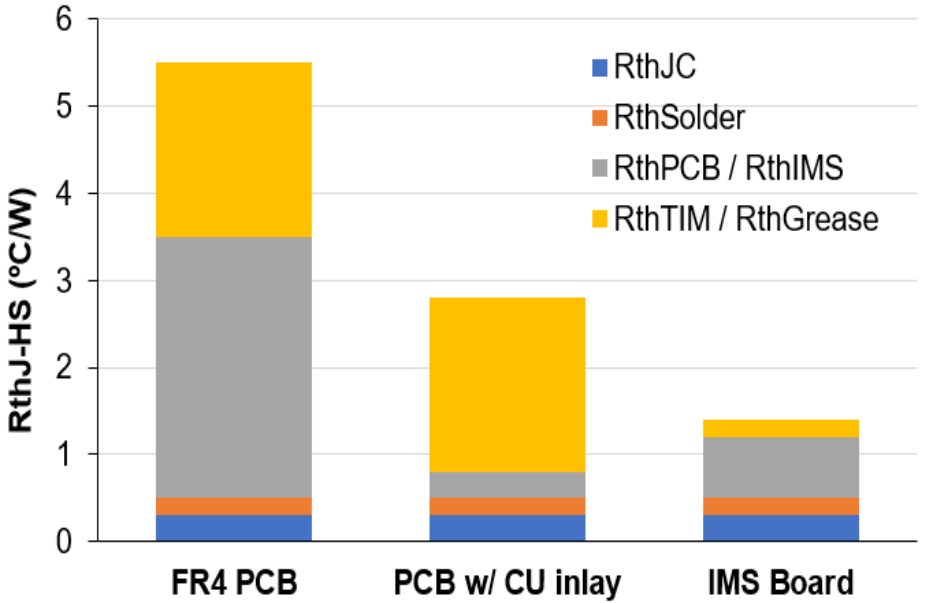
- Gate driver board design concept
- Assemble on top of IMS(metal core) boards

- More compact layout and lower stray inductance than traditional power module, optimized for high speed GaN
- Thermal resistance $\mathbf{R_{thJC}}$ **~= 1℃/W**

The thermal performance is enhanced compared with the PCB solution.

Reference Design of 240A/650V GaN Module





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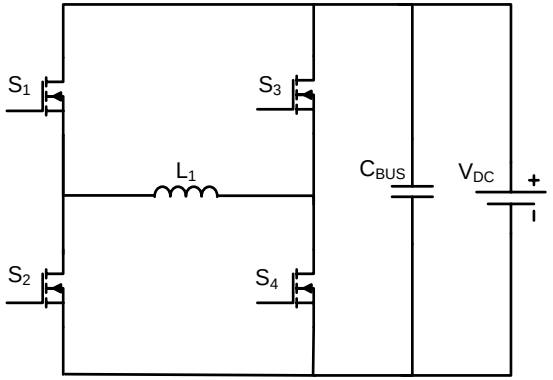
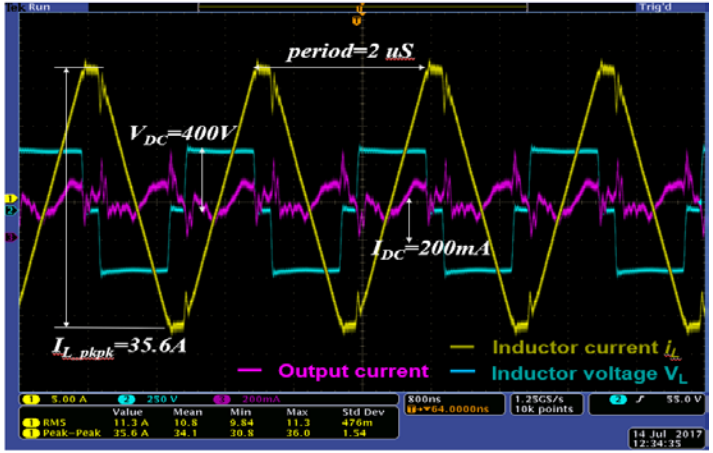
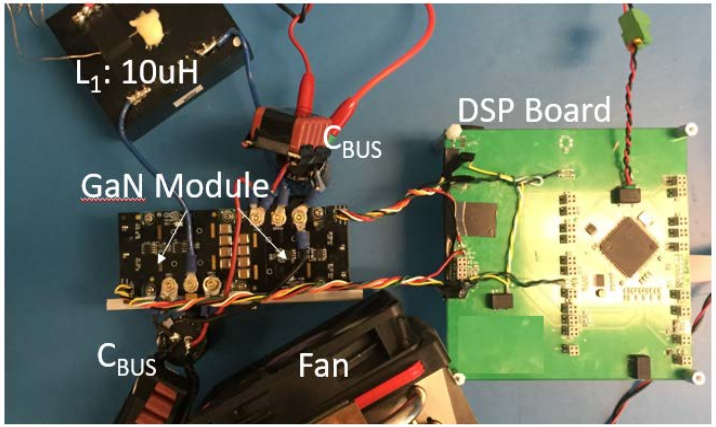
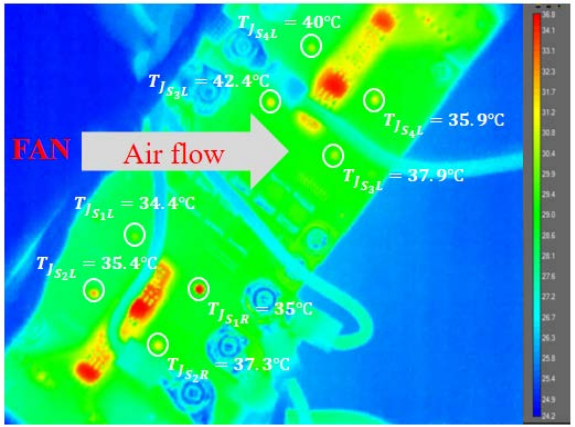
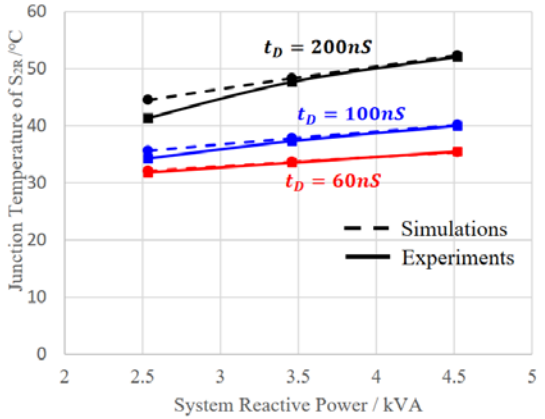
Experimental Results











Thank you!
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Any questions?