Agenda

- Basics
- Gate Drive Design considerations
- Design examples
- PCB Layout
- Switching Testing results

Latest update JAN-18-2018
Please visit http://www.gansystems.com/whitepapers.php for latest version of this document
GaN Enhancement mode High Electron Mobility Transistor (E-HEMT)

- Lateral 2-dimensional electron gas (2DEG) channel formed on AlGaN/GaN hetero-epitaxy structure provides very high charge density and mobility.
- For enhancement mode operation, a gate is implemented to deplete the 2DEG underneath at 0V or negative bias. A positive gate bias turns on the 2DEG channel.
- It works just like MOSFET except better switching performance.

![Diagram of GaN HEMT](image)
E-HEMT Gate characteristics

Common with Si MOSFET
- True e-mode normally off
- Voltage driven - driver charges/discharges $C_{iss}$
- Supply Gate leakage $I_{GSS}$ only
- Easy slew rate control by $R_G$

Differences
- Much Lower $Q_g$ : Lower drive loss; faster switching
- Higher gain and lower $V_{GS}$ : +5-6V gate bias to turn on
- Lower $V_{G(th)}$: typ. 1.5V

Versus other e-mode GaN
- More robust gate: +7/-10V DC max rating
- No DC gate holding current required
- No complicated gate diode / PN junction

<table>
<thead>
<tr>
<th>Gate Bias Level</th>
<th>GaN Systems GaN E-HEMT</th>
<th>Si MOSFET</th>
<th>IGBT</th>
<th>SIC MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum rating</td>
<td>-10/+7V</td>
<td>+/-20V</td>
<td>+/-20V</td>
<td>-8/+20V</td>
</tr>
<tr>
<td>Typical gate bias values</td>
<td>0 or-3/+5-6V</td>
<td>0/+10-12V</td>
<td>0 or -9/+15V</td>
<td>-4/+15-20V</td>
</tr>
</tbody>
</table>
Reverse Conduction Characteristics

- No body diode, but 2DEG can conduct in 3rd quadrant – **No need for anti-parallel diode**
- When gate is OFF (during dead time), 2DEG exhibits like a diode with $V_F = V_{th} + V_{GS(off)}$
- Reduce dead time loss: 1) minimize dead time; 2) Use smaller or avoid negative $V_{GS}$ if possible
Reverse recovery performance

Reverse Recovery charge $Q_{RR}$:

- GaN has zero $Q_{RR}$ making it suitable for **half bridge hard switching** – Replace IGBT
- Si MOSFET can’t be used for any half bridge hard-switch circuit due to $Q_{RR}$
- Excellent reverse recovery of GaN enables new topologies such as bridgeless totem pole PFC

Half bridge turn-on 400V/20A – SJ MOSFET

Si MOSFET $Q_{RR}$ Loss = 6670uJ!

Half bridge turn-on 400V/20A – GaN E-HEMT

Math: $V_{DS} \times I_D$

Snappy recovery:
1. High $di_{RR}/dt$, parasitic ringing
2. Body diode ruggedness

Qoss Loss only:
1. Much lower turn-on loss
2. No snappy recovery and uncontrolled high $di_{RR}/dt$
3. Clean waveforms
Setting up dead time

- For hard switching: $t_{d\_pwm}$ must be $> t_{\text{delay\_skew}} + (t_{d\text{(off)}} - t_{d\text{(on)}})$:
- Gate turn-on/off delay difference varies with $R_G$: typical +/-5ns range (GS66508)
- High/low side gate driver delay skew (worst case delay mismatch) usually dominates:
  - Example Silab Si8261 isolated gate driver $t_{\text{delay\_skew\_max}} = 25$ns. In this case the dead time must be set $> 30$ns as minimum
  - However in practical circuit safety margin must be considered: for GS66508 typical 50-100ns is chosen for dead time
- For soft switching dead time needs to be chosen for achieving ZVS transition
- For 100V: smaller can be used (10-20NS) as 100V driver has better delay matching

![Diagram](image)

Actual dead time $T_{d\_actual} \approx t_{d\_pwm} - t_{\text{delay\_skew}} - t_{d\text{(off)}} + t_{d\text{(on)}}$
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Design Considerations – fast switching

GaN switches faster than Si/SiC MOSFETs with $dv/dt > 100\text{V/ns}$

- GaN shows 4x faster turn-on and ~2x faster off time than state of art SiC MOSFET with similar Rds(on)

**Double Pulse Test Hard Switch Turn-on**

(V$_{DS}$=400V, I$_D$=15A, R$_{G(ON)}$=10Ω)

- GaN E-HEMT GS66508T (650V/50mΩ)
- Cree SiC C3M006509D (900V/65mΩ)

- V$_{gs}$=12V/-3V (SiC)
- V$_{gs}$=6V/-3V (GaN E-HEMT)

- 4.5ns (90V/ns)
- 17ns (18V/ns)

**Hard Switching Turn-off** (V$_{DS}$ = 400V, I$_D$ = 15A, R$_{G(OFF)}$=1Ω)

- GaN E-HEMT
- SiC

- V$_{gs}$=12V/-3V (SiC)
- V$_{gs}$=6V/-3V (GaN E-HEMT)

- 5.7ns
- 10ns
Design Considerations

Design considerations for driving high speed GaN E-HEMTs:

**Controlling noise coupling from power to gate drive loop should be the first priority:**

- High $dv/dt$ and $di/dt$ combined with low $C_{iss}$ and $V_{G(th)}$ $\rightarrow$ Need to protect gate spikes from going above threshold or maximum rating under miller effect for safe operation
- Gate ringing or sustained oscillation may occur if the design is not done properly and may lead to device failure. We will discuss how to mitigate that in this section
- On the other hand, the switching performance of GaN should not be compromised too much
- This is more critical for 650V hard switching half bridge application as very high $dv/dt$ could occur at hard turn-on.
- Single end topology has less concern with miller effect, and for resonant ZVS topology the $dv/dt$ and $di/dt$ are lower so their design requirement may be relaxed.

In this section we will walk through the design tips on how to control miller effect and mitigate gate ringing/oscillation, followed by gate driver recommendations
Gate drive impedance (Rg and Lg) is critical for turn-off, but less at turn-on.

**Basic rule:** the gate needs to be held down as strong as possible with minimum impedance.

Miller effect is more prominent at 650V than 100V design due to the higher dv/dt.

### Positive dv/dt

- Prevent false turn-on
- Strong pull-down (low R_G/R_{OL})
- Low L_G to avoid ringing
- Use negative gate bias, -2 to -3V is recommended

### Negative dv/dt

- Occurs at turn-on of the complementary switch in half bridge
- Keep V_{GS-\_pk} within -10V
- Strong pull-down (low R_G/R_{OL}) and low L_G for lower ringing
- V_{GS} may bounce back >0V (LC ringing): ensure V_{GS+\_pk} < V_{G(TH)} to avoid false turn-on or gate oscillation
Control Miller Effect

- For negative dv/dt, it is important to have a low-Z path for the reverse miller current to reduce the negative $V_{GS}$ spike (and the ringing afterwards caused by LC resonance)
  - Pay attention to the $V_{GS}$ spike around $V_{DS} < 50V$ due to the change of non-linear $C_{ISS}/C_{RSS}$ ratio
  - A clamping diode is recommended for gate drive with single output. For gate drive with separate sink output the diode may not be needed depending on the $R_G$ and $L_G$ in the circuit
  - For bipolar gate bias, use a TVS diode in series with the clamping diode (or two back to back)
  - $C_{GS}$ may not help in some cases, be careful! (induce LC resonance with $L_{gate}$ and $L_{CS}$)
  - Negative gate bias can help to prevent false turn-on, but ensure worst case $V_{gs-\_pk}$ within -10V
Control miller effect

Select right gate resistor

- GaN E-HEMT speed can be easily controlled by gate resistors
- Critical to choose the right $R_{G(ON)}/R_{G(OFF)}$ ratio for performance and drive stability
- Separate $R_G$ for turn-on and off is recommended
- Recommend $R_{G(ON)}/R_{G(OFF)} \geq 5$-$10$ ratio for controlling the miller effect
- GaN has extremely low $Q_g$ and drive loss: most cases 0402/0603 SMD resistors can be used
- Turn on $R_{G(ON)}$:
  - Control the turn-on $dv/dt$ slew rate
  - Too high $R_{G(ON)}$ slows down switching and increases loss
  - Too small $R_{GON}$: High $dv/dt$ -> Higher switching loss due to the miller turn-on and potential gate oscillation
  - For GS66508: recommend to start with $R_{G(ON)} = 10$-$20\Omega$
- Turn off $R_{G(OFF)}$:
  - Typical starting value range is $1$-$2\Omega$
  - Provide strong and fast pull-down for robust gate drive
Mitigate gate ringing/oscillations

What causes the gate ringing/oscillation?

- Gate over/undershoot and ringing caused by high $L_G$
- Common Source Inductance $L_{CS}$ Feedback path from power to gate loop ($\text{di/dt}$)
- Capacitive coupling via miller capacitor $C_{GD}$ ($\text{dv/dt}$)
- Noise coupling via test probe

What to do if gate ringing/oscillation occurs?

- First improve the layout by reducing $L_G$, $L_{CS}$ and external G-D coupling:
  - Locate driver as close to gate as possible
  - Low inductance wide PCB trace and polygon
  - Use kelvin source connection to minimize $L_{CS}$
- Select right $R_G$ to tune turn-on slew rate
- Try negative gate bias (-3V) for turn-off
- At last resort try circuits below to damp the high frequency LC ringing & overshoot:
  - Use a ferrite bead with $Z=10-20\Omega$@100MHz in series with gate. (ferrite bead may increase $L_G$ but damp the high frequency gate current ringing)
  - RC snubber across G-S: example $R=3.3/C=200-470\text{pF}$
High side driver considerations

High side gate drive

- **GaN enables fast switching dv/dt > 100kV/us:**
  - Minimize Coupling capacitance $C_{IO}$
  - CM current via $C_{IO}$ limits CMTI
  - Use isolator/isolated gate driver with high CMTI

- **Full Isolated gate drive:**
  - Best performance
  - Isolation power supply – Minimize inter-winding Capacitance

- **Bootstrap:**
  - Common for lower voltage 100V half bridge design
  - Lower cost and simpler circuit
  - *Choose the bootstrap diode with low $C_J$ and fast recovery time. Watch for bootstrap diode power loss limit and recovery time for high-frequency operation.*
  - Post-regulation or voltage clamping may be required after bootstrap

Optional common mode choke at input side to suppress CM noise
Bootstrap circuit

- Good for low cost 0-6V gate drive
- What is the problem with traditional bootstrap circuit?
  - GaN E-HEMT requires good regulation of gate bias (5-6V bias, max rating 7V)
  - LS free wheeling: Switch node negative voltage overcharges bootstrap capacitors (V_{GS}>7V)
  - HS free wheeling: Bootstrap diode voltage drops reduces V_{GS} below 6V
- Post-regulation or voltage clamping to ensure high side bias is tightly regulated to 6V

Bootstrap with post-regulation using +9V for regulated high side bias
Use LDO to regulate to 6V

Bootstrap for Sync Buck (only need to clamp overcharge, example 100V sync buck)
Simple Zener diode to clamp to 6V
## Recommended GaN driver/controller ICs

Following drivers have been verified by GS and are recommended for design with our GaN E-HEMTs:

<table>
<thead>
<tr>
<th>Configurations</th>
<th>Gate Driver/Controller IC</th>
<th>Design resources</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>650V Half/Full Bridge:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. DC/DC: LLC, PSFB, Sync Boost/Buck</td>
<td>Si8271 – Single; Si8273/4/5 – HB/Dual -GB (0-6V) or –AB (-3/+6V)</td>
<td>Si827x Datasheet Si8271 demo board (GS66508T) IMS evaluation board User Guide</td>
</tr>
<tr>
<td>2. AC/DC: Totem pole PFC, Active Clamp Flyback</td>
<td>ADuM4121ARIZ (0-6V Drive) ADuM4121BRIZ (-3/+6V Drive)</td>
<td>ADuM4121 Datasheet</td>
</tr>
<tr>
<td>3. Inverter, motor drive</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>80-100V Half/Full Bridge</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. 48V DC/DC</td>
<td>LM5113(NRND): 100V, max 5MHz</td>
<td>LM5113 Datasheet</td>
</tr>
<tr>
<td>2. 48V POL</td>
<td>LMG1205: 80V/5A HB Driver</td>
<td>LMG1205 Datasheet</td>
</tr>
<tr>
<td>3. Sync. Buck/Boost</td>
<td>PE29101: 100V, 48V DC/DC, 33MHz</td>
<td>PE29100 Datasheet PE20102 Datasheet PE29102 Demo board (GS61004B)</td>
</tr>
<tr>
<td>4. Class D Audio</td>
<td>PE29102: 60V, Class D Audio, WPT, 40MHz</td>
<td></td>
</tr>
</tbody>
</table>
### Recommended GaN driver/controller ICs

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<tr>
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| **Low side non-isolated driver for 650V/100V GaN**:  
1. Flyback, Push-pull  
2. Forward  
3. Boost PFC  
4. Secondary SR  
5. Class E P/A | LM5114/UCC27511: Single Channel, 4A, 5-6V drive  
UCC27611: w/ internal LDO (5V) |  
LM5114 Datasheet  
UCC2751x Datasheet |
|                                                      | uP1964: Internal LDO for 6V drive                      | uP1964 Datasheet                       |
| Other GaN compatible drivers                     | IXD609SI: Single, 6V drive, high drive current (9A)  
FAN3122/TC4422: Single, 6V drive, high drive current (9A)  
FAN3223/4/5: Dual 4A, 6V drive, for push-pull or SR application | |
| **Sync Buck DC/DC (100V GaN)**                   | LTC7800: 60V, Sync. Step-Down Controller (up to 2.2MHz, w/ integrated GaN compatible drivers) | LTC7800 Datasheet                      |
| **Secondary side Rectification (100V GaN)**      | NCP4305A: 5V gate drive clamp, 1MHz max               | NCP4305 Datasheet                      |
| 1. High frequency LLC  

[*] – low side non-isolated drivers can also be used on high side / half bridge configurations by combining with level-shift / signal isolators, see [page 29](#) for design example.
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650V Isolated Driver Design #1 – 0-6V drive

Si8271-based isolated driver (0-6V drive)

- VDD: 5/9 or 12V depending on system power rail
- Optional CM Choke for better noise immunity against dv/dt
- Choose isolated DC/DC PS1:
  - 5/9/12V to 9V, 1W, 3kV isolation
  - Low Cio preferred for dv/dt immunity
  - Verified/Recommended P/N:
    - RECOM R1S-xx09/HP
    - Mornsun Fxx09XT-1WR2
- PWM Input:
  - 3.3V or 5V logic from controller
  - Optional RC filter for noise filtering
  - Consider driver w/ deglitcher (-IS1 suffix) for noisy environment
- Enable:
  - Direct tie to VDDI if not used
  - Recommend filter cap (100nF) close to EN pin to prevent false triggering

6V LDO for tight VDRV regulation

Recommended for high-frequency ZVS application

Gate resistors:
1. Turn-on RGATE R2: typ. 10-20Ω
2. Turn-off RGATE R3: typ. 1-2 Ω
650V Isolated Driver Design #2 – bipolar drive

Si8271-based isolated gate driver (-3/+6V drive)

- Lower risk of cross-conduction and gate oscillation, faster turn-off (lower switching loss)
- Higher reverse conduction loss
- Recommended for hard-switching or high power applications

DZ1 and R2 divide 9V into -6V and +3V gate bias. The mid-point is used as a ground 0V which should be connected to the SS of GaN device

- Place bypass cap C7/C8 close to U1 VDD/GND
- Keep loop between U1 and Q1 Gate/SS as tight as possible
- Higher UVLO driver can be used
Use fast recovery low $C_J$ diode for Bootstrap:
- C3D1P7060Q
- UFM15PL
- ES1J

LLC test waveform (400V/1.3A 600kHz)
ADuM4121ARZ-based isolated gate driver for GaN HEMT (0-6V drive)
Isolated gate driver based on ACPL-P346 (-4/6V)

Half Bridge Board Reference Design
GaN Systems 650V E-HEMT **GS66508T** (30A/50mΩ) transistor
Broadcom 2.5A gate drive optocoupler, **ACPL-P346**
[https://docs.broadcom.com/docs/ACPL-P346-RefDesign-RM101](https://docs.broadcom.com/docs/ACPL-P346-RefDesign-RM101)
**100V half bridge GaN driver – PE29101**

- 80V HB driver for GaN
- Support 6V gate drive
- 48V DC/DC application
- High frequency (>5MHz)
- Dead time adjustable
- Small low inductance Pkg

PE29102 - 60V HB GaN driver optimized for high frequency applications:
- Class D Audio, DC/DC and wireless power charging

Non-isolated low side driver for GaN

- For single-ended applications (Class E, Flyback, Push-pull etc), or
- Used to adapt MOSFET gate drive bias to 5-6V drive for GaN (low or high side)

LM5114 low side driver

9-12V Aux power

From controller logic signal (3.3/5V) or MOSFET driver output (up to 14V)

uP1964 GaN Driver

- integrated regulator for 6V bias
- 5V LDO
Non-isolated low side driver for GaN

Isolated GaN driver for high side / half bridge using low side driver + signal isolator or HB driver
- Overcome frequency and drive performance limit of previous isolated driver solution
- Adapt to existing controllers/half bridge driver (ensure the driver is capable of handling high dv/dt)
- Improved gate drive loop by locating LS driver close to GaN

5V for isolators

Place U4 close to Q1 and keep the loop tight
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Innovative packaging for high speed GaN device:

- Extremely low inductance: high frequency switching
- Near Chip Scale embedded Packaging
- No wire bonding: high reliability
- Better CTE match to PCB: Temp cycle reliability*
- Lower thermal resistance $R_{\text{thJC}}$

[*] GaNPx passed 1000hr IPC9701 solder joint reliability test, condition: 12-Layer 2.5mm PCB, 5oz inner copper and 2oz outer copper.
PCB Layout Checklist

- Design for GaNPx embedded package
  - GaNPx bottom cooled B/P
  - GaNPx Top cooled
  - Thermal design

- Optimize and minimize layout parasitics in following orders:
  1. Common source / mutual inductance $L_{CS}$
  2. Gate loop inductance $L_G$
  3. Power Loop inductance $L_{loop}$
  4. Drain to gate loop capacitance $C_{GD\_ext}$
  5. Isolation coupling capacitance $C_{ISO}$
GaNPx™: Bottom cooled B type family

- Embedded package with extremely low inductance
- GS66508B includes dedicated kelvin source pin (SS)
- PCB cooling using thermal pad (S) and vias or metal core PCB for high power application

**GS66508B (650V, 30A, 50mΩ)**

- Embedded package with extremely low inductance
- GS66508B includes dedicated kelvin source pin (SS)
- PCB cooling using thermal pad (S) and vias or metal core PCB for high power application

**GS66504B/GS66502B (650V, 15/7A, 100/200mΩ)**

- GS61004B (100V/45A, 15mΩ)

**Create Kelvin source on PCB**

**Use SS pin for gate return**

**Create Kelvin source on PCB**

**Gate Return**

**Main Current Flow**
**GaNpx™**: Bottom cooled P type

- Similar to B type except substrate (thermal pad) is floating on the package
- Use SS pin for kelvin source connection
- **The thermal pad must be always connected to its source pin on PCB**

**GS61008P (100V/90A, 7.5mΩ)**
Layout best practice – Gate Drive

1. Use/create kelvin source to separate drive return and power ground (low $L_{CS}$). Physically separate high current loop and drive loop areas to minimize noise coupling.

2. Minimize pull-down loop (Gate → R3 → U1 → C2 → GS_RTN, locate U1 and C2 close).

3. Minimize turn-on (pull-up) loop (locate C1 close).

4. Isolate and avoid overlap between gate drive and Drain copper pour.

5. Isolate and avoid overlap from Drain/Source to the control grounds (CMTI, dv/dt).
Layout best practice – Gate drive with Top-cooled package

1. GaNPx T package located at bottom side for heatsink attachment

2. Create kelvin connection to the source for Gate drive return (bottom side)

3. Use multiple vias for lower gate inductance from bottom to top side

4. Use one gate and keep the other floating
Design the half bridge power stage with tight loop and low inductance

**Layout guidance**
- Recommend to use 4-Layer PCB
- Use 2\textsuperscript{nd} layer as ground return
- Use SMD MLCC decoupling caps and locate them close to GaN
- Use multiple decoupling caps to reduce ESR/ESL and create balanced power loop
- Locate drivers close to the gate
- Use kelvin source for driver return
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Switching Test – GS66508B Half bridge Eval board

- PWM Signal/+5V VCC connector
- Si8271GB Isolated drivers
- Decoupling Capacitors
- Isolation Barrier
- VGS probe
- Recommended Switching node probe position for Eon/Eoff measurement
- Optional current shunt
  Use copper foil to short if not used
Double pulse switching test

- GS66508B hard switched up to 400V/30A

![Diagram showing a circuit with labels for VDS, VGS, IL, VGL, and VDC+ with a waveform graph showing Inductor current IL, VDS, VGS, and VGL with annotations for VDS=400V, ID=30A, RGON=10Ω, RGOFF=1Ω.]
GS66508 Double pulse switching test

$V_{DS}=400V, I_D=30A$ Hard Switching Turn-on

$V_{DS} = 400V$

$V_{GS}$

Clean $V_{GS}$ waveforms

Estimated Loop inductance = 3nH

Peak turn-on $dv/dt=80V/ns$

VDS dip due to loop inductance: $\Delta V=Lp*di/dt$

Peak turn-on $dv/dt=80V/ns$

Clean rising edge w/ low Vds overshoot (low loop inductance)

$V_{DS}=400V, I_D=30A$ Hard Switching Turn-off

$I_L = 30A$

$V_{DS}$ peak = 450V

Peak Turn-off $dv/dt>100V/ns$

$\tau_r = 3.9ns$

Estimated Loop inductance = 3nH
Summary

- This application guide summarized the key design considerations for GaN Systems GaN E-HEMTs. We started with the fundamental aspects of GaN E-HEMTs and then the gate drive design considerations were discussed. A list of recommended drivers and several gate drive reference designs were provided.

- The second part of this guide focused on the PCB layout and discussed the layout best practice by using GaN Systems Embedded package GaNPx.

- At last a real half bridge evaluation board design following the design recommendations in this document was built and its switching performance was tested.

- The switching test results showed fast and clean hard switching waveforms up to full rated current 400V/30A with minimum ringing/overshoot. This concluded that with optimum gate drive and board layout combined with low GaNPx inductance, GaN E-HEMTs exhibit optimum switching performance.
Design resources

- PCB Footprint libraries: http://gansystems.com/design_library_files.php
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